APPLICATION NOTE

AN01

Camera Electronics for the mK x nK CCD Image Sensor Family

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Abstract

This application note is a comprehensive document written to develop a full understanding of the mK x nK CCD image sensor family and to help design a digital CCD camera with true 12-bit performance.

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AN01

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Summary

Since the introduction of the first mK x nK CCD family there has been a growing need for detailed application information. This application note fulfills this need by giving comprehensive information that will help customers design with any member of the mK x nK CCD family. Besides some CCD theory it provides very useful information on how to design a high performance digital camera that will get the most out of the CCD.

The design notes are for many kinds of application with any mK x nK CCD family member. They are valid for the FTF3020 (which is recognized as the standard in professional digital photography), the FTT1010 (for general and high-speed imaging) and others.

Chapter 1 provides the reader with some basic CCD theory plus some specific details regarding the mK x nK CCD family. The information presented is the minimum that an electronic engineer should be aware of when designing a CCD camera.

Chapter 2 details all aspects that are specific for this CCD family. The topics are Frame Transfer CCD, Full Frame CCD, sensor layout and read-out modes. Good knowledge of these items is a must to discover the possibilities and limitations of the various devices.

Chapter 3 presents a reference design including a lot of in-depth design considerations, hints and warnings. The design is a result of years of experience in camera electronics design for all kinds of applications including digital photography, broadcast and medical imaging.

Chapter 4 summarizes all critical issues the camera design engineer should be aware of. Anyone who really wants to build a high performance camera should read this chapter (and follow the rules).

History

Document	Status:	Date	Author
AN01-R1	Initial release	03-03-1999	E. Herijgers
AN01-R2	Change: horizontal binning	18-02-2000	P. te Vaarwerk
AN01-R3	Transfer to DALSA	22-04-2002	F. Polderdijk

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1 CCD basics

1.1 Charge handling

1.1.1 Potential Well

Each pixel is covered by 4 gates. These gates influence the behavior of a pixel. Depending on the applied gate voltage, an electron well (bucket) or electron barrier forms underneath the gate. Our mK x nK sensors are buried channel devices combined with an anti-blooming feature. Buried channel means that the accumulated electrons are stored beneath the silicon surface, so that they cannot be trapped easily by the Si-SiO_2 interface. Anti-blooming means that if a bucket is completely filled with electrons, additional generated electrons are drained to the silicon substrate instead of spreading to neighboring pixels.

The well works like a bucket which gets filled with water. When the bucket is almost full and more water is poured into the bucket, water is drained to the substrate. Underneath a barrier gate no electrons (water) will be accumulated.

Figure 1 shows the potential in Volts versus the depth in the substrate. Curve 1 represents an empty well under a positive biased gate during integration. Electrons generated in the upper part of the silicon will be collected in the potential well, electrons generated deeper will disappear into the n-type substrate. Holes disappear into the p-well. A blocking gate or barrier gate is biased during integration at 0V, as depicted by curve 2. The small potential well underneath this gate is responsible for an active barrier gate. This means that electrons generated underneath the barrier gate will be collected into neighboring potential wells. If all gates of the image cells are biased to 0V, there will no longer be any potential well in the silicon, and no electrons can be stored. Curve 3 shows this situation. Biasing all gates to -5V as shown in curve 4 can reinforce this behavior of a pixel.

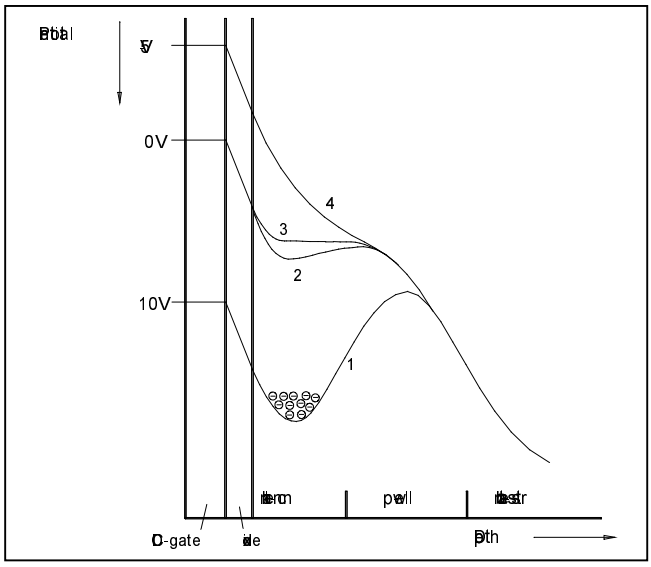


Figure 1. Potential Well Diagram

The behavior of a pixel is not only influenced by the gate voltage, but also by the DC-voltages on the n-substrate (VNS) and on the p-well (VPS). At default, VPS and VNS are set to their typical voltage levels as given in the data sheet. To optimize the sensor performance VPS is kept at this value while VNS can be changed. A higher VNS-voltage leads to better anti-blooming performance, but decreases the well capacity and slightly decreases the light sensitivity. On the other hand a lower VNS-voltage increases the well capacity, but lowers the anti-blooming performance. The optimal adjustment is achieved, when VNS is set as low as possible, while at the same time proper anti-blooming is still guaranteed.

1.1.2 Integration

Integration takes place in the image area only. Each pixel is covered by 4 gates (gates A1 to A4). Applying the typical integration and hold level to one of the gates means the bucket is formed under this gate and electrons can be accumulated. In other words, the pixel is integrating.

When the typical low voltage level is applied to a gate, this gate forms a barrier in the silicon and is therefore blocking. The typical integration and hold levels for each sensor can be found in the corresponding data sheet.

To form a cell, neighboring pixels have to be separated from this cell. Channel stops prevent electrons from moving to the left or to the right, thus forming the pixel boundaries in the horizontal direction. Vertically, one gate is set to its low voltage level and is blocking the electrons from moving up or down this column. The other three gates are set to the typical integration and hold level during integration.

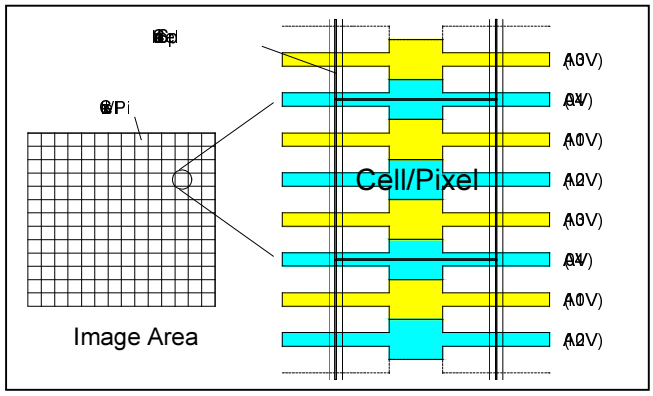


Figure 2. Cell/Pixel Definition

Some applications may require integration under two gates instead of three. This leads to a loss in sensitivity and maximum charge handling capability, but increases the vertical MTF performance. The changes in the timing are not discussed in this application note, but can easily be derived from the presented information.

1.1.3 Charge Storage

To store the charge of a pixel the same principal is used as for integration. When the typical integration and hold level is applied to the gate, a well forms underneath this gate, the typical low voltage level forms an active barrier.

It is possible to use only two blocking gates, because they can store the complete amount of charge when the image gate voltages are increased (to 14V typical). However, the dark current increases if higher voltage levels are applied to the gates. More than two blocking gates should not be used, because it would leave just one storing gate which cannot store the charge packet of a full image pixel well.

1.1.4 Charge Reset or Electronic Shutter

Charge Reset (CR) is often called electronic shutter when it is used to shorten exposure times. The charge, which is already integrated, can be dumped to the substrate by a charge reset procedure to start a new integration period. This can be accomplished in two ways:

1. *Switching the low level of the image gates.*
   Set all image gates at the same time to the typical charge reset level. The following figure shows this situation.

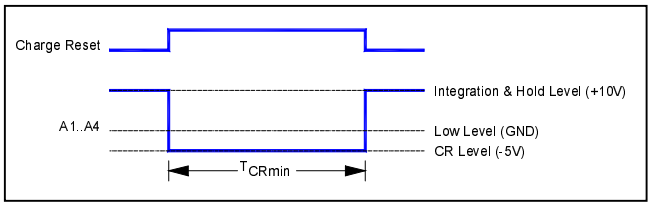


Figure 3: Charge Reset on image gates

2. *Pulse on VNS*.
   Set all image gates at the same time to the typical low level, while a CR-pulse is applied on top of the n-substrate voltage.

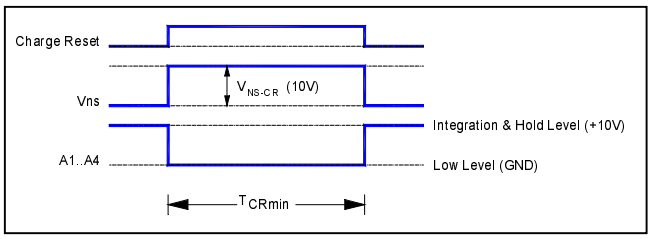


Figure 4: Charge Reset on N-substrate

Either way the minimum charge reset duration should be at least the minimum charge reset time.

The main criteria for selecting a charge-reset method are the CCD type and the application needs. From the driving electronics point of view, the second method is preferred. However, the first method has the advantage of connecting some capacitors directly to VNS resulting in a more solid by-passing. However, the performance of both methods is equal. CR on the image gates is necessary when using a frame transfer CCD in real-time mode (that is, simultaneous integration and read-out) because a pulse on VNS cannot be used since this pulse will affect the charge in the storage area (refer to chapter 2 for an introduction to CCD types).

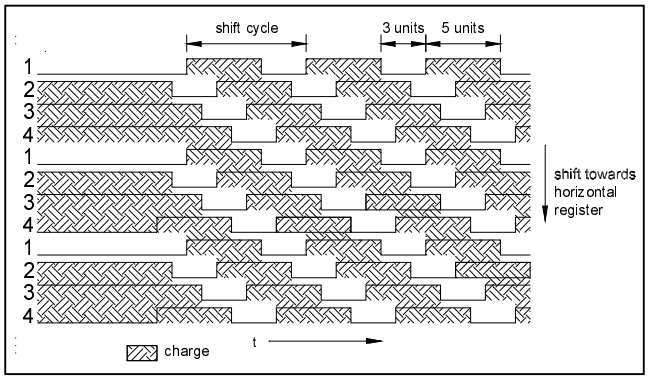
Another important issue in this mode is that the charge reset should be done within the line blanking, because the charge dumped to the substrate will affect the read-out of the image in the storage area. Charge reset should always be applied before each integration cycle to empty the image completely from eventual remaining charges. This eliminates possible smear generated during the previous frame transport (for a FT CCD) and sets each frame to the same state at the beginning of an integration period.

1.2 Charge transport

1.2.1 Vertical Charge Transport

Transporting the charge packets is done by controlling the high and low voltage levels of the image/storage gates. The vertical charge transport can be compared to the movement of a caterpillar. Figure 5 shows the operation of this process. To reach a sufficient overlap during the vertical transport, a duty cycle of 5:8 is used. This means that for 5 units the pulse is high and for three units it is low. The delay from one to the next pulse is 2 units or 90°.

Figure 5: Vertical Charge Transport



An important issue of charge transport is the amount of overlap. The charge should be at least under two gates. Overlapping is reduced by too slow rise and fall times of the transport gate control voltages. This results in a transport efficiency penalty that leads to a lower Q_{max}. Therefore it is essential to use drivers which are capable of driving the CCD with the specified rise and fall times. To achieve the typical well capacity Q_{max}, it is necessary to transport the charge no faster than the typical transport speed as specified in the data sheet. Exceeding the maximum frame transport frequency decreases Q_{max} considerably.

1.2.2 Line Transport

During a line transport sequence, one line from the image or storage area is shifted into the horizontal register (C-gates) during the line-blanking period. The shift mechanism is the same as used for the vertical charge transport, changing the gate voltages from low to high and vice versa.

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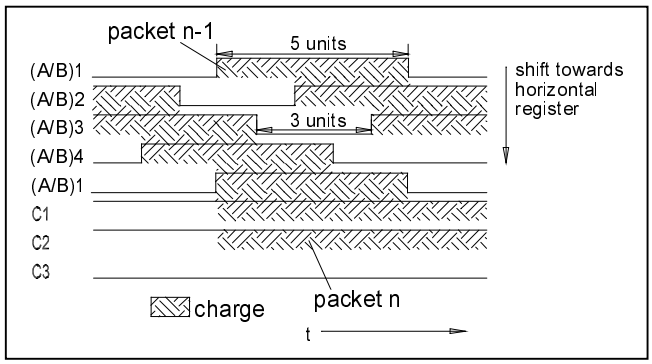


Figure 6: Line Transport / Vertical Transport of 1 Line

The columns are separated from each other by blocking gate C3 during line transport. This means that the horizontal register receives the charge packets under the gates C1 and C2 when the line transport takes place.

When the last image/storage gate goes low, the charge is completely shifted into the horizontal register. When the C-clocks start running, the charge packets are shifted towards the output amplifier(s).

1.2.3 High Level switching

CCDs are capable of transporting charge at integration and hold levels. However, using an increased voltage swing (0-14V) during vertical charge transport leads to a better transport capacity and is therefore necessary to obtain the performance as specified in the data sheet. The low voltage levels remain at the typical low voltage level. The following figure shows high level switching during line transport.

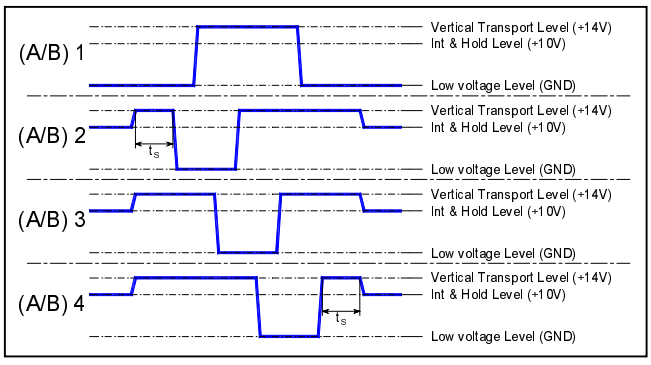


Figure 7: High level switching during line transport

At the start of the horizontal blanking the high levels are switched from 10V to 14V. The actual vertical transport is allowed to start a short time (t_s) after the high levels are settled to 14V. A short time (t_s) after the moment the gates are settled to their initial values (and the transfer is completed), the high levels are allowed to switch back to 10V. The time t_s must be greater than or equal to 1/8th of the vertical frequency period.

1.2.4 Horizontal Transport

The horizontal transport is only discussed for the default output register which delivers the normal view (not mirrored) of the image. The maximum transport frequency is given in the data sheet. The duty cycle used for the horizontal transport is 3:6 (or 50%). This means that for 3 units the pulse is high; for the other 3 units it is low. The delay from one to the other pulse is 2 units or 120°.

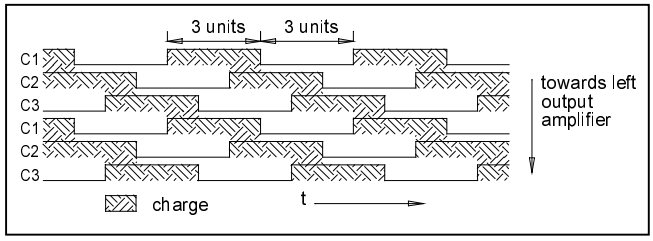


Figure 8: Horizontal Transport towards Left Output Buffer

Changing the gate voltages in a certain order forces the charge packets to move to the left or right. For each clock cycle the charge packets move exactly one register cell towards the output buffer. To shift the packets to the right output buffer (mirror view), the pulses on gate C1 and C2 should be interchanged. Like the vertical transport, fast rise and fall times are crucial for obtaining maximum charge transport efficiency. The essence here is that the time that the charge packets are under two adjacent gates should not be too short (overlap). Refer to the data sheet for maximum rise and fall times.

1.2.5 Output Buffer and CCD Output Signal

The output gate (OG) is connected to a DC bias voltage. The output gate forms a potential barrier that allows the electrons to flow to the floating diffusion (FD) only when the last gate is set to its low level. In the case of the mK x nK family the last gate before the floating diffusion is a summing gate (SG), which enables horizontal binning possibilities (see section 1.3).

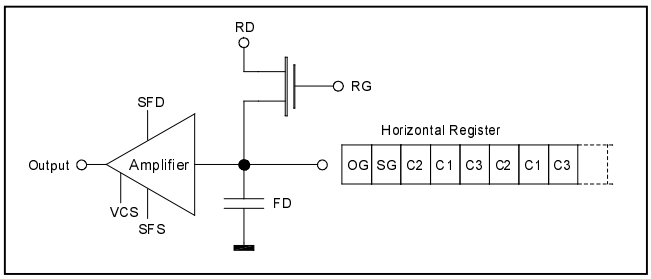


Figure 9: Functional View Output Buffer, Floating Diffusion, and Horizontal Register

The data sheet defines the DC bias voltage levels and voltage swings of the C-pulses and the summing gate (SG). The output buffer is a three-stage source follower with an open source output (which makes an external resistor necessary). The floating diffusion converts the charges into a voltage swing, which is buffered by the output buffer. SFD is the positive supply voltage of the source follower, SFS the negative supply voltage. VCS controls the current sources of the first and second source follower stage of the buffer and is mostly connected to GND.

The reset gate (RG) input pin is connected to a MOS-transistor gate. If RG is high, the charge on the floating diffusion is drained towards the reset drain (RD) potential. The pulse on RG is derived from the C-pulses. It has a width of approximately 1/6 Tp (T_{RG}).

Timing of the RG-pulse in relation to the SG-pulse and C-pulses is very critical and needs a carefully designed circuit.

When no horizontal binning is applied, the summing gate waveform is identical to C3. The electrons are drained before a new charge packet is dumped on the floating diffusion (SG goes low). The reset gate pulse causes cross-talk on the output signal of the CCD (see section 3.3.5 on pre-processing). The RG pulse leads, in conjunction with the SG pulse, to a duty cycle of the video signal of 50%.

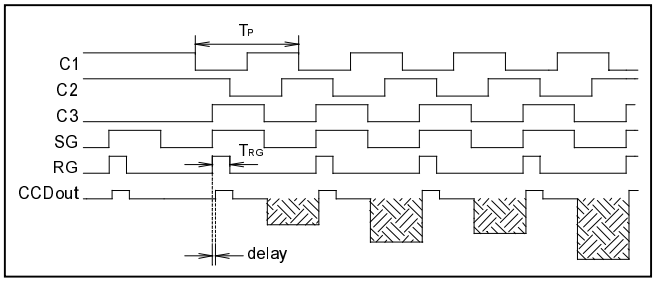


Figure 10: The Reset Gate Pulse

The output signal of the CCD is depicted schematically in Figure 10. It shows a short delay in comparison to the pulses RG and SG. This delay is caused by the output buffer (the value is approximately 5ns).

The output signal of the CCD is depicted in Figure 11 as it can be seen on an oscilloscope. It has to be processed by a pre-processing circuit to eliminate noise and demodulate the video signal. The signal can be divided into three main parts; the cross talk with the reset gate pulse, the reset hold level, which is used by each pixel as a zero electron reference for the pre-processing and the actual video signal.

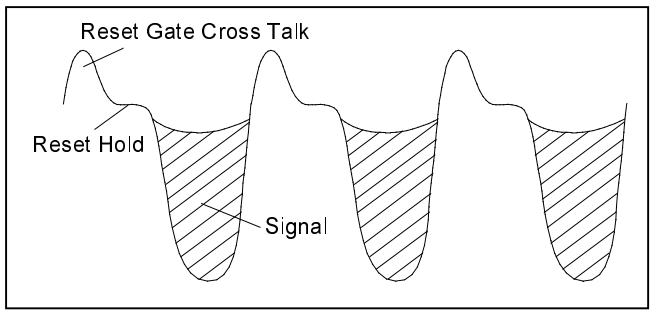


Figure 11: CCD Output Signal

1.3 Binning

Definition of binning: combining two (or more) pixels into one pixel. Binning can be useful when a higher read-out speed or more sensitivity is desired while a decrease of resolution is acceptable. A possible disadvantage of applying binning in a CCD is the danger of exceeding Qmax (in highlights) resulting in blooming effects.

Binning is supported vertically and horizontally. Binning can be carried out vertically by shifting two (or more) lines into the horizontal register during the line blanking period instead of only one. After the line transport is completed, the horizontal shift transports the charge packets to the output buffer.

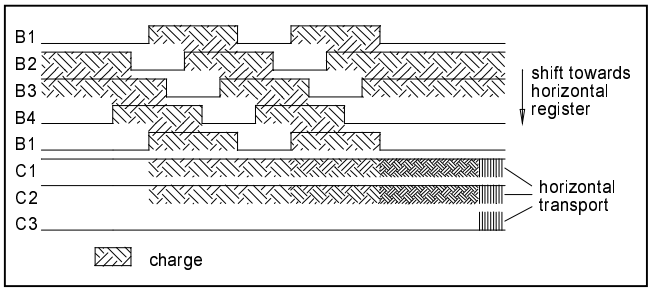


Figure 12: Vertical Pixel Binning

The summing gate (SG) is used for horizontal pixel binning. When horizontal binning is used the readout speed will not be affected (read-out speed stays the same).

To reset the floating diffusion a Reset Gate (RG) has to be applied, This can be done in two ways:

Option 1: The reset gate (RG) pulse is applied to every other pixel, so that two charge packets can be shifted underneath the summing gate while it is kept high. When the summing gate goes low, the charge of two packets flows to the floating diffusion. The RG pulse is chosen in such a way that the duty cycle of the actual video signal is again 50%.

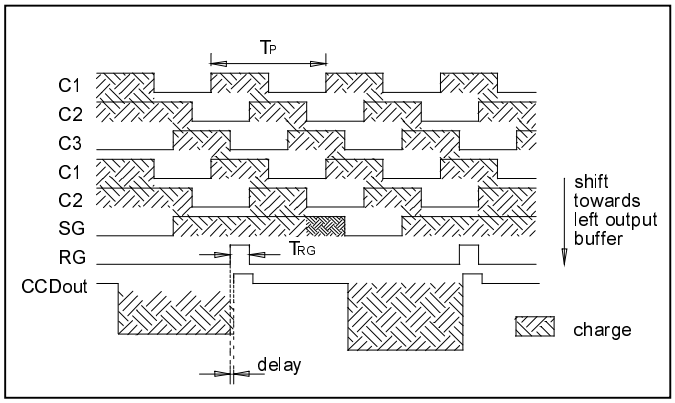


Figure 13: Horizontal Pixel Binning option 1

A disadvantage of option 1 is when charge-packets become too large it is possible that charge will flow over the output gate and come on the floating diffusion. Then there is no proper hold level.

Option 2: To avoid the disadvantage of option 1 you can use option 2. The RG pulse has its original frequency, see figure 14.

This option is ***preferred.***

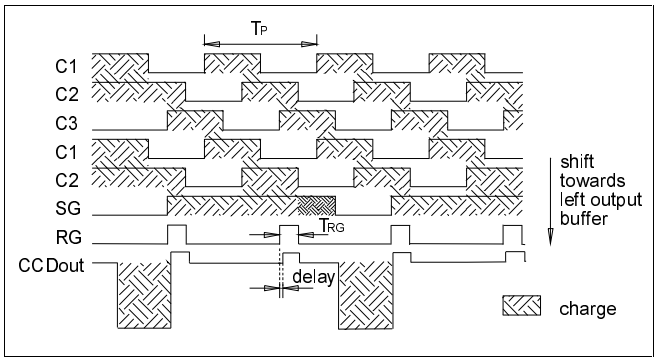


Figure 14: Horizontal Pixel Binning option 2 (preferred)

If the CCD is used in a digital camera, another way of horizontal binning may be adding two subsequent pixel values in the digital domain. This eases the (critical) hardware design of the horizontal clocks. When using digital binning the danger of blooming doesn't exist.

Binning in a color CCD will mix up colors.

2 The mK x nK CCD sensor family

2.1 Frame Transfer and Full Frame Imagers, an Introduction

2.1.1 Frame Transfer CCD

The frame transfer device consists of four functional parts:

1. Image area
2. Storage area
3. Horizontal registers
4. On-chip amplifiers

The location of each of these parts is shown in Figure 15.

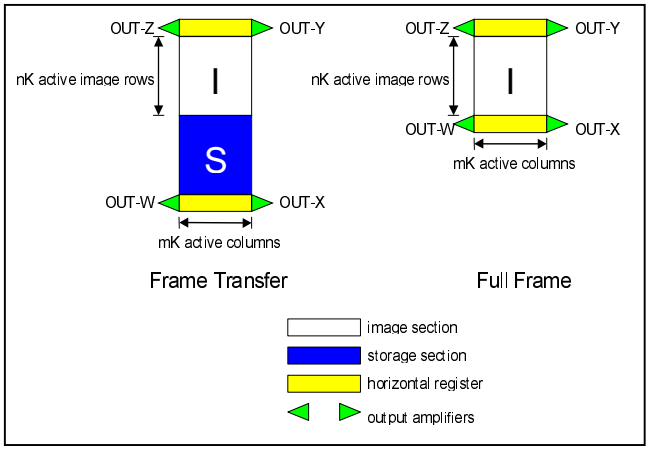


Figure 15: Functional diagram of mK x nK CCD

The frame transfer device is able to capture an image and to transfer it to the storage part of the sensor, where it is protected from further exposure to light. Afterwards the storage section can be read out without significantly corrupting the data by continued exposure. In comparison to the transfer the read-out is a slow process. The corruption of data by continued exposure is called smear. The amount of smear results from the relation of frame-transport time to integration time. Wider FT and FF devices can only be driven at lower frame-transport frequency. This results in a lower frame rate and read-out speed due to higher gate capacitance's. When integration of the next field begins, the stored image information is transported into the horizontal register line-by-line (in parallel) and then read out (in serial) through the output amplifier(s).

2.1.2 Full Frame CCD

The full frame device consists of three functional parts:

1. Image area
2. Horizontal registers
3. On-chip amplifiers

The location of each of these parts is illustrated in Figure 15.

In a FF CCD the captured image is not transferred into a storage area, but is read out through the one or two registers directly. While reading out the image line-by-line through the top and/or bottom horizontal output register and pixel-by-pixel through the left and/or right output buffer, the image area has to be shielded from light so that no further integration takes place. To avoid smear the image area should be illuminated with strobed light or used with a shutter in the optical path, so that the read-out takes place without further exposure to light. After the read-out is finished the sensor is exposed to light again and the next image can be read out.

2.1.3 Possible transport directions

By clocking the gates of the FT or FF imager it is possible to read out an image in many different ways. The possibilities for transporting an image are illustrated in Figure 16.

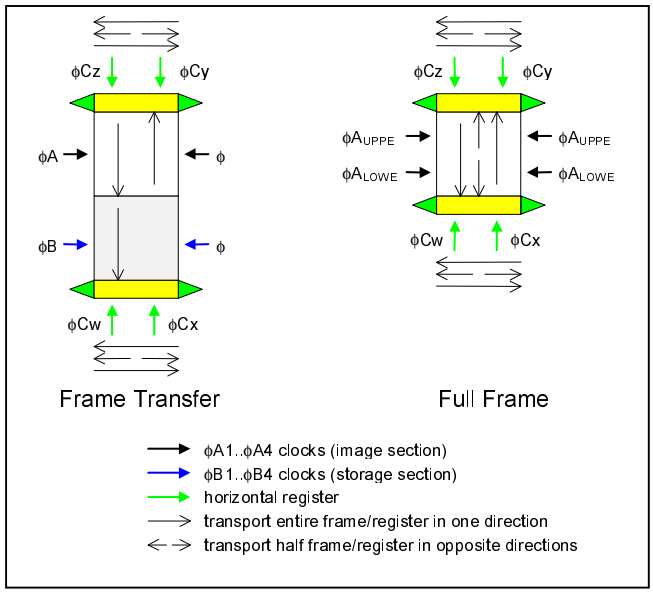


Figure 16: Possible transport directions

Frame Transfer: The entire image can be transported to the storage section (Frame Transport, a quick process) or to the upper horizontal register (slower process, due to the fact that each transported line has to be read out).

Full Frame: The entire image can be transported to the upper or lower horizontal register or the upper half of an image can go to the upper register and the lower half to the lower register.

Both types of sensors have an output amplifier on each end of the horizontal register. So the image can also be read entirely through one amplifier (left or right) or split between the two. All four amplifiers can read a quarter of the image (FF only), or two can read half, or one can read an entire picture. In other words, the image of a FF sensor can be split along two axes (one horizontal and one vertical) and the image of a FT sensor along one (vertical). But both can also be treated as a continuous array across the midlines.

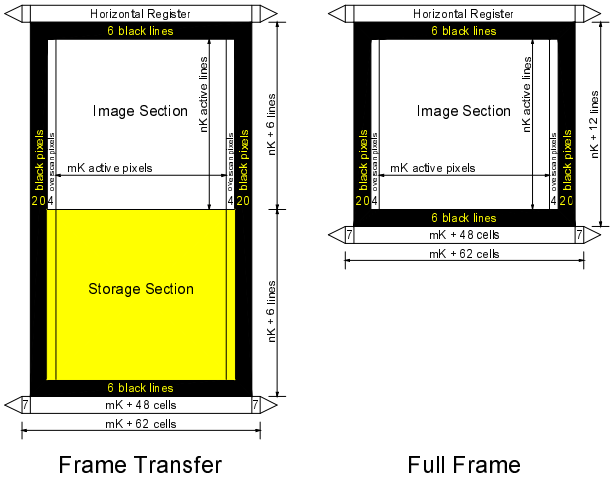
As Figure 16 shows, the possibilities for the frame transfer device are even greater. For example, two pictures can be taken with only a small time between them by snapping one, transporting it under the storage shield, snapping a second and reading both out at the same time after protecting the image area from light.

2.2 Sensor Layout

Where the previous section only gave a general description of the mK x nK CCD family, this section goes into more detail. To design an application with one of the family members it is necessary to fully understand the items presented in this chapter. Being aware of the gate arrangement is important to create the correct waveforms and to know exactly at what time each specific pixel will be read out through the output amplifier(s).

2.2.1 Physical Layout

The exact arrangement of the functional parts is described in this section. Figure 17 shows the physical layout of both the Frame Transfer and Full Frame devices.



Note that the horizontal registers, black lines, black and overscan pixels are not drawn to scale in comparison with the size of the image and storage section.

Figure 17: Physical layout FT and FF CCD

The black colored lines and columns can be used for generating the black reference that is necessary in subsequent video processing circuits for the restoration of the video black level. The four columns on both sides next to the mK x nK image area are overscan pixels and are not shielded from light. Their behavior is identical to the active image area pixels. Note that these eight columns do not count in the mK image columns.

2.2.2 The transport gates

A mK x nK sensor in general has several leads to control image/storage transportation and the horizontal read-out of an image. This chapter explains the function of those gates which are most important for the transport functions and the read out of images.

The horizontal transport gates of each quadrant are independently wired from each other (see Figure 18) and can be controlled separately. The vertical transport gates are also independently wired, but are electrically connected in the middle of the sensor. This means that the top half (Z+Y) and the bottom half (W+X) of the sensor can be controlled separately. This allows FT devices to read out 2 outputs simultaneously while FF devices can even read out 4 outputs simultaneously.

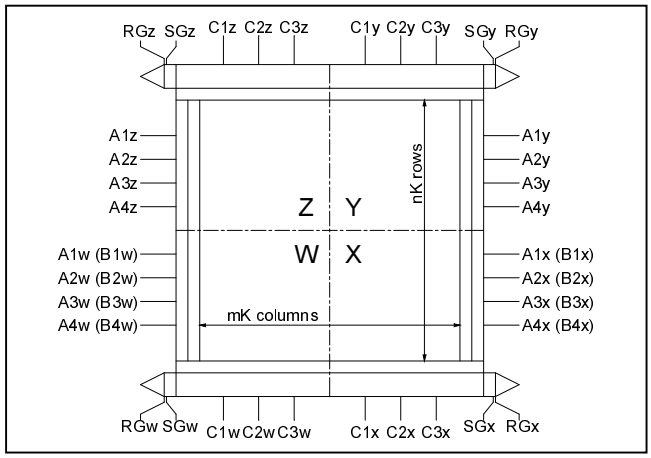


Figure 18: Schematic view of transport gate leads

The difference between the Full Frame and Frame Transfer device is that in FT sensors areas W and X are shielded by aluminum (storage section and black columns) and each controlled by B gates (names between brackets).

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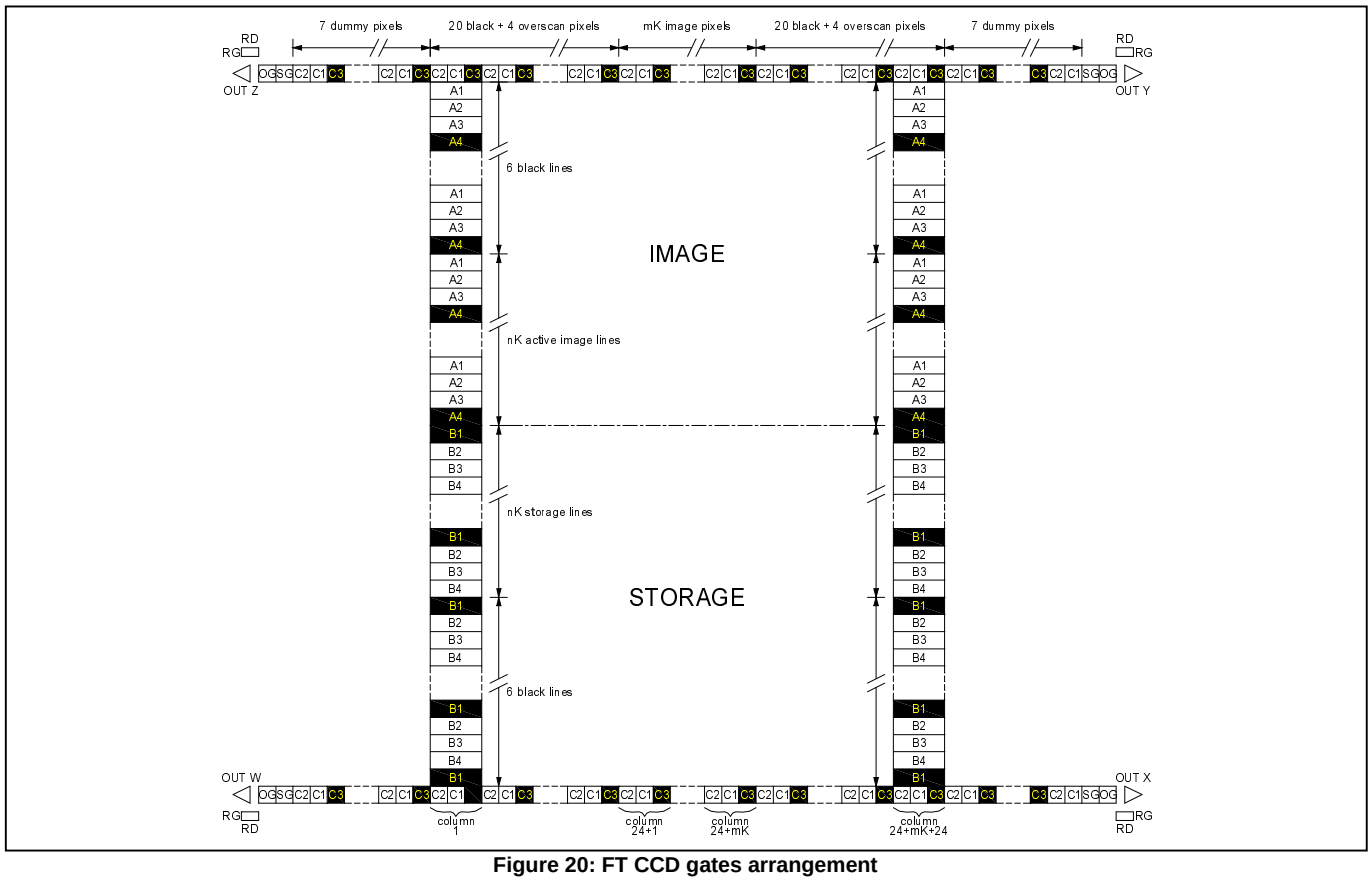

Figure 20: FT CCD gates arrangement

Figure 20 illustrates how the gates in a mK x nK FT sensor are arranged and where the gates are positioned.

The black colored gates in Figure 20 separate the pixels in the vertical direction in the image and storage section during integration and in the horizontal direction in the registers during the transport of a line into a register.

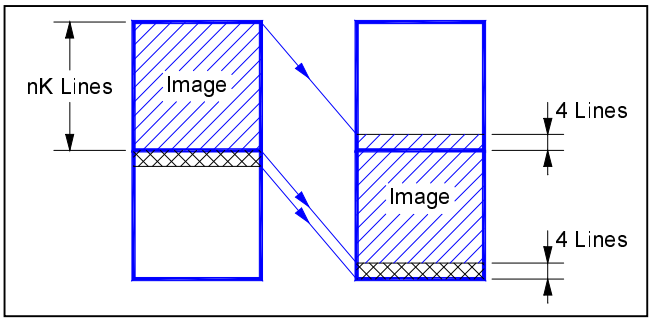

Figure 19: FT black reference lines

To achieve a reasonable black level restoration, some specific issues must be taken into account. The border of the shielding is between the image and storage area. This means that no black reference lines are available at the bottom of the image.

Black reference lines can be created by shifting not the complete image down into the storage, but shifting only the total number of lines minus 4. Figure 19 shows this process.

By shifting nK lines minus 4, the last 4 lines are not read out. Instead, the 4 lines at the bottom of the storage are dummy lines that are created during the read-out of the last four lines of the previous image. When reading out the next image, the first four lines (which in fact are dummy lines) can be used to restore the black level.

A consequence of this operation is that it is necessary to make the last image gate (A4) the blocking image gate in order to create the dummy lines.

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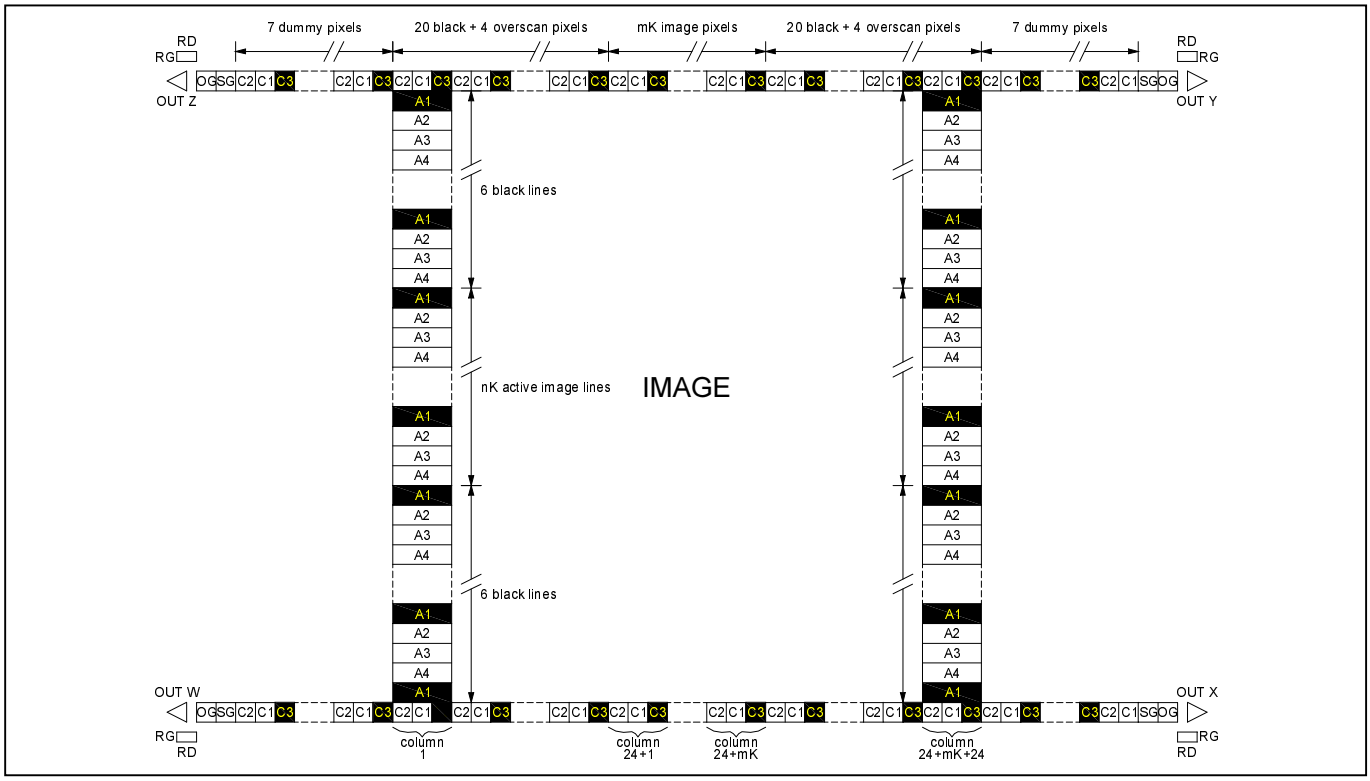


Figure 21: FF CCD gates arrangement

Figure 21 shows the gate arrangement from a FF CCD. In this case A1 is the blocking gate.

Figure 22 shows the vertical line of symmetry through a mK x nK sensor. Note that the horizontal registers have one more gate on the left side than on the right, so that the vertical line of symmetry in a horizontal register is through the middle of the C3 gate in the middle of the register.

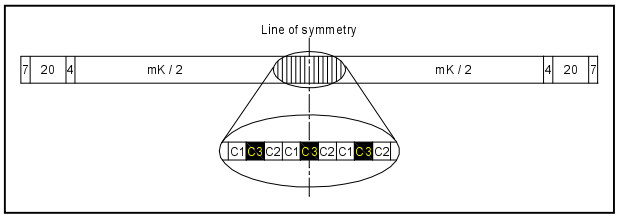


Figure 22: Vertical line of symmetry

2.3 Using multiple outputs

Most applications require only one CCD output. However, if the frame rate is an important issue, the mK x nK CCD family has the ability to read out through 2 or even 4 output amplifiers simultaneously. This section explains the consequences of using multiple outputs on the output sequences.

2.3.1 Dual Output Mode (FT and FF)

Normally when using a single output the picture is read out through output W. The read-out speed can be doubled by using two outputs instead of one. In this situation the image is vertically split up into two halves.

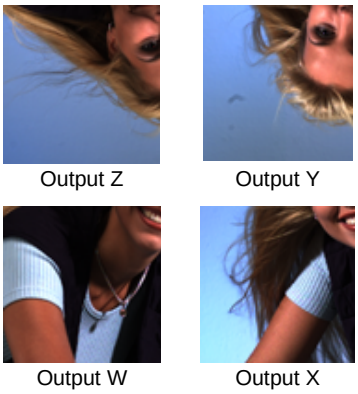
Single output (W) Dual output (W) Dual output (X)

Figure 23: Single and Dual output FT or FF CCD.

Instead of successive reading out mK active pixels each line, both the outputs read out mK/2 active pixels simultaneously. Note that the X output mirrors the image in horizontal direction as shown above. Before processing the X output sequence should be restored (for example, using a FIFO buffer) to the normal order.

2.3.2 Quad output mode (FF only)

In comparison to the double output mode the frame rate can again be doubled by using four outputs. This is only possible with Full Frame devices. In this case the image is also split up horizontally. A quarter of the image will be read out through each output amplifier.



Output Z Output Y

Output W Output X

Figure 24: Quad output FF CCD

In this situation output Z is mirrored in vertical direction, output X in horizontal direction and output Y in both directions as shown above. Restoring the original sequence requires a frame buffer of at least half the image size.

3 Reference Design: Digital CCD Camera

3.1 Introduction

This chapter details the actual camera design. It is full of schematics and design considerations for designing a good quality CCD camera.

It is assumed that the reader is familiar with the basic CCD basics and terminology, presented in the previous chapters, and all general mixed signal design issues.

The schematics are valid for an FTT1010 at 20MHz pixel-rate, but most of it can also be applied to larger CCDs such as the FTF3020. Design notes are included to adapt the electronics for other frequencies and/or CCD types.

Although the presented electronics are thoroughly tested in our application lab and in several other applications, don't expect to start mass production immediately after the first PCB layout design. In most cases it is necessary to refine the design to your own needs specific for each application. Remember that this note is primarily meant to provide customers with the necessary knowledge and hints to design their own camera.

All component types and manufacturers used in this camera design are listed in Appendix 1.

3.2 Design Overview

This section explains the building blocks described in this chapter. The following block diagram shows the global relations between the functional blocks.

The camera is supplied with a clean symmetric 6V and a single +15V supply. To prevent cross-talk from digital power supply lines to the analog ones, all are separately stabilized using low-drop regulators. The 15V input is used to create all CCD bias supply voltages as well as the image/storage high-level voltages. Most of the bias supply voltages are derived from the VSFD regulator. As the block diagram shows, the most central part is the Pulse Pattern Generator (PPG). It controls most of the other blocks and has some feedback signals to turn off the CCD bias supply voltages and the image/storage clocks if current limit is sensed on one of the CCD bias voltages.

A free-running oscillator generates the pixel clock. The duty cycle is settled to 50% by a feedback loop. The horizontal clock shaping logic creates the necessary delays and pulses for the CCD, pre-processing and A/D conversion. All of these signals are buffered and some of them are boosted in amplitude. One of the clocks is used to clock the PPG. The main function of the PPG is to drive the high-level and low-level switches and the vertical drivers. It also drives the charge pump inside the 29V generator, the horizontal clock shaping logic and the digital output buffer (to be connected to a frame grabber). The CCD output signal is buffered and pre-processed by means of a discrete-built CDS circuit coupled to an A/D converter.

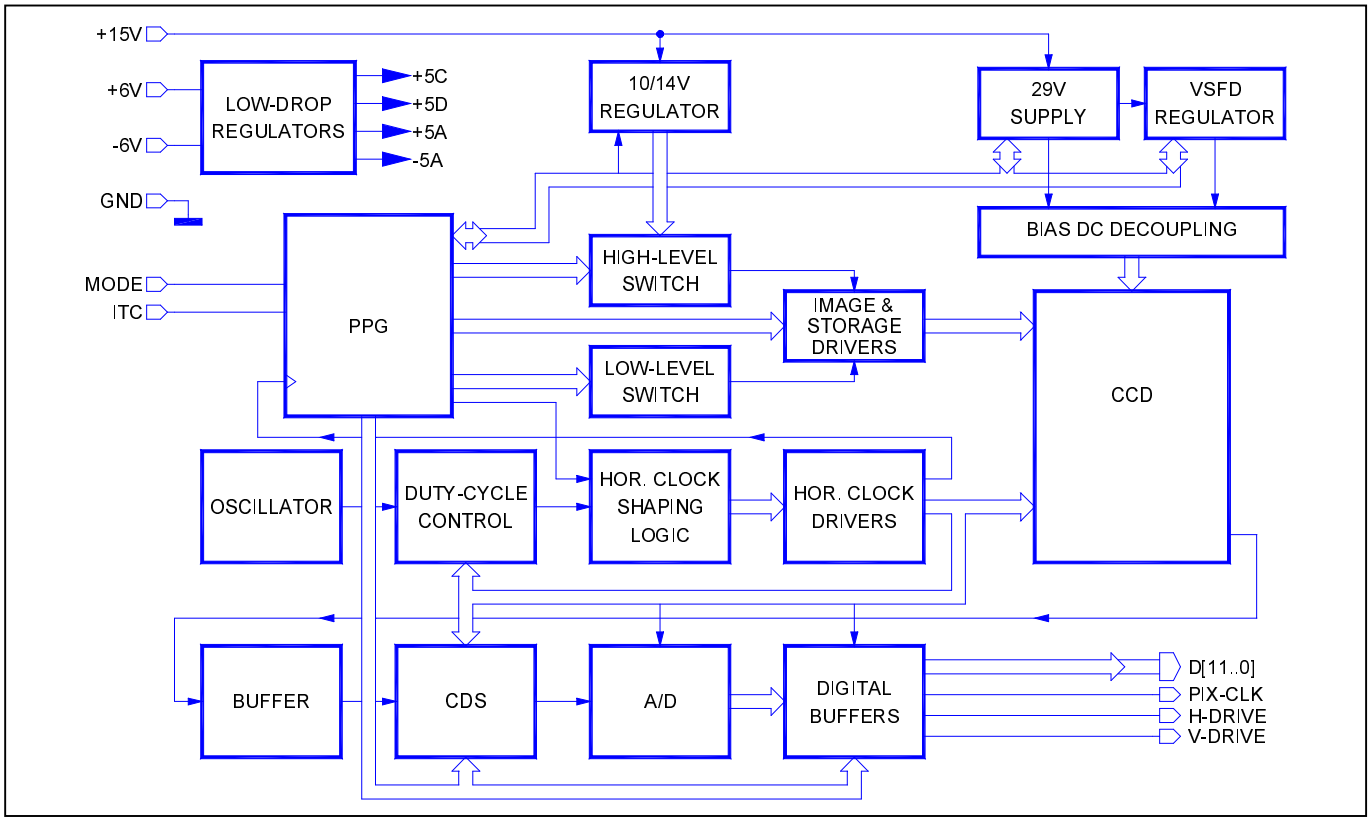


Figure 25: Block diagram

3.3 Detailed Description

3.3.1 DC Bias Supply

3.3.1.1 29V Supply

The highest DC voltage necessary for operating a CCD sensor is the Nsub voltage (VNS), which is in most cases within a range of 24..27V. Therefore 29V is sufficient to supply VNS as well as the SFD voltage and all other sensor DC bias voltages. Figure 26 shows an example of a 29V supply circuit.

The first stage boosts the input voltage from 12V to approximately 40V by means of a charge pump. Two pulses called SCP+ (not inverted) and SCP- (inverted) control this charge pump. The frequency of these pulses is half the line frequency (each pulse is toggled during the line blanking). Two level-shifter/drivers are used to boost the (TTL level) pulses to 12V amplitude.

Before the voltage is stabilized to 29V the ripple is suppressed with a second order filter followed by a current sense circuit. The output (29V-LIM) is used to switch off the SCP pulses when the current exceeds the value set by R1 (for example, when the 29V is short circuited). Switching off the SCP pulses prevents the regulator from break down as a result of too much power dissipation. Chapter 3.3.4 explains all the details of the protection circuitry throughout the camera.

The final stage is the 29V regulator. The output current is limited to approximately 40mA by TS1 and R2. Although it is built with discrete components, an integrated type could also be used.

Design considerations

The output voltage of the charge pump circuit depends on the frequency of the charge pump pulses, the output impedance of the drivers, and the size and quality of the capacitors. In particular a low Equivalent Series Resistance (ESR) value is of great importance. (ESR acts like a resistor in series with a capacitor and degrades the capacitor's effectiveness as a by-pass element.) In order to make sure that the current sense feedback (29V-LIM) operates as it should, it's threshold should be set to a lower value than the threshold of the regulator (thus, R1 < R2). With a short-circuit of the output, the SCP pulses are always switched off, resulting in a lower power consumption of the regulator and preventing the emission of smoke.

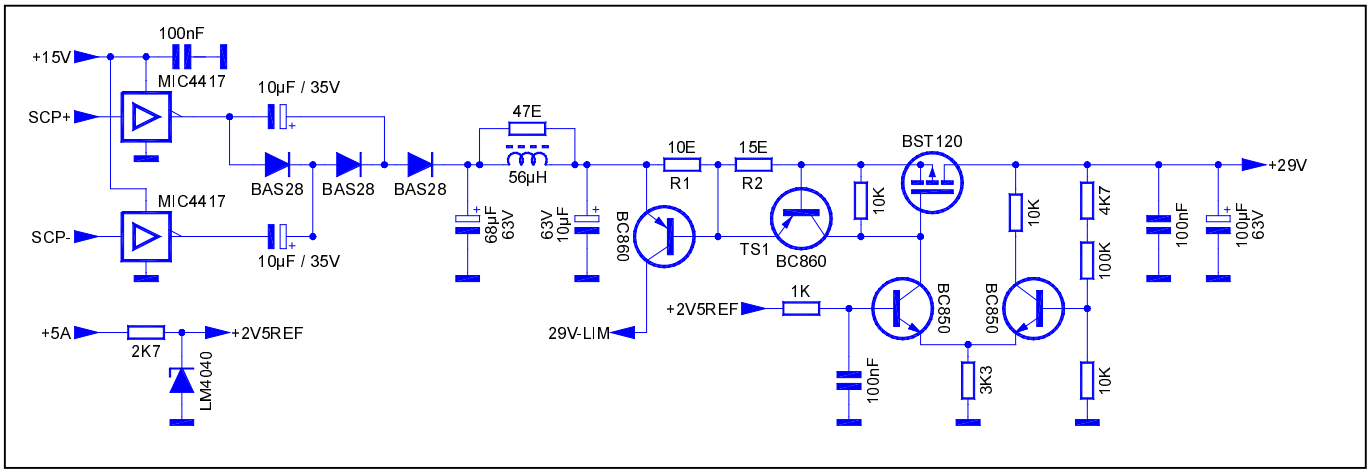


Figure 26: 29V Supply

3.3.1.2 VSFD Regulator

The second regulator in the DC bias circuit is the VSFD regulator. This regulator is used to supply the output buffer(s) of the CCD (named SFD) and the emitter follower(s) mentioned in paragraph 3.3.5.1. It is further used to tap some other bias voltages that the sensor needs (RD, PS, OG, C1 to C3, RG and SG).

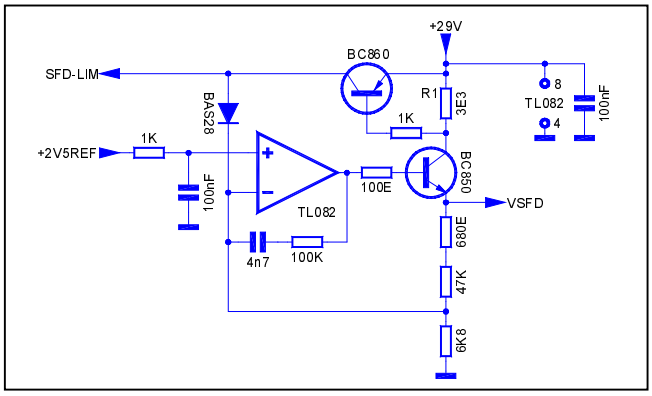


Figure 27: SFD Regulator

Operation of this circuit is straightforward. The reference voltage is amplified and buffered. If the output current exceeds the value set by R1, the output is cut off and the current limit output (SFD-LIM) is pulled up. Refer to chapter 3.3.4 for all details of the protection circuitry throughout the camera.

3.3.1.3 Bias DC By-passing

The Nsub supply is tapped from the 29V. After buffering (which is not necessary for smaller sensors like the FTT1010) each quadrant is separately by-passed with 100nF capacitors. When no charge reset is applied to VNS the circuit in Figure 28 can be used.

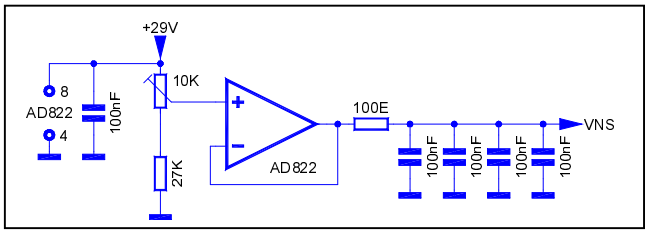


Figure 28: Nsub supply without CR on Nsub

If charge reset should be applied to VNS, some components should be added as shown in Figure 29. The CR-NS signal is driven by the PPG (see section 3.3.3.1).

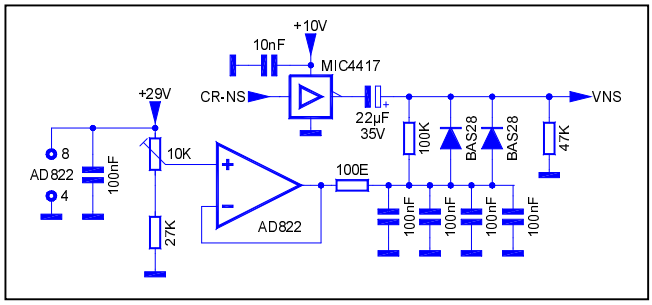


Figure 29: Nsub supply with CR on Nsub

The RD and PS supplies are tapped from VSFD. PS is buffered (in large sensor applications) and each quadrant is separately by-passed with 220nF capacitors. The RD pin of each quadrant is connected via a 100K/100nF low-pass filter. Figure 30 shows the RD / PS supply. Notice the four Schottky diodes that are used to protect the sensor against unwanted potential differences that may damage the CCD and make it useless. Section 3.3.4 gives detailed information about this issue.

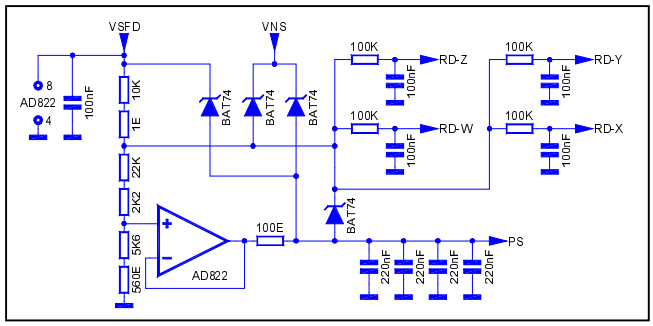


Figure 30: Reset Drain / Psub supply

The OG voltage is tapped from VSFD and distributed to each OG pin via a 100K/100nF RC filter. Again, each quadrant has its own by-pass capacitor.

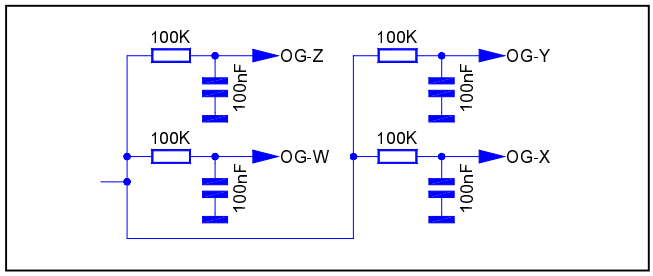


Figure 31: Output Gate supply

The bias voltages of the gates C1 to C3, SG and RG are all tapped from VSFD. Chapter 3.3.2.4 shows how these bias voltages are connected.

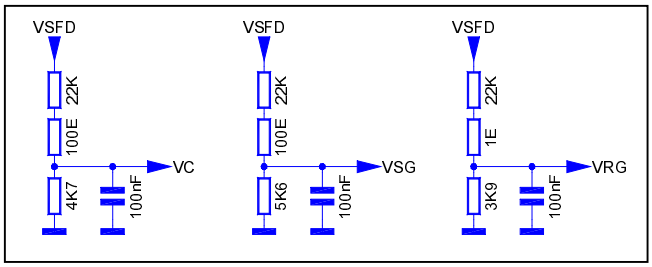


Figure 32: C1 to C3, Summing Gate and Reset Gate bias voltages

3.3.1.4 10V/14V Regulators

A ripple free 15V is necessary to create 10V and 14V to feed the high level switches for the image (and storage) gates. Figure 33 shows the 10V and 14V regulators plus a common protection / disable circuit.

Each regulator consists of two MOSFETs controlled by an Op-Amp that compares the tapped output with a reference voltage (REF). A RC combination is used to slow down the start-up speed of the regulator outputs. Pulling the REF signal down can shut down the regulators. There are two sources that can disable the regulators. The first is the current sense circuit and the second is the signal AB-DISABLE. This signal goes high when something happens with the 29V or VSFD. This is detailed in section 3.3.4 about protection circuits.

When using a FT CCD a current buffer (R1/C1) at the input of the 14V regulator is necessary to smooth the input current (caused by the vertical transport). When using a Full Frame CCD a smaller capacitor (±100µF) is sufficient. However, a larger capacitor (having a lower ESR value) improves ripple suppression.

Any ripple on the 14V during the active line read-out will become visible in the output signal.

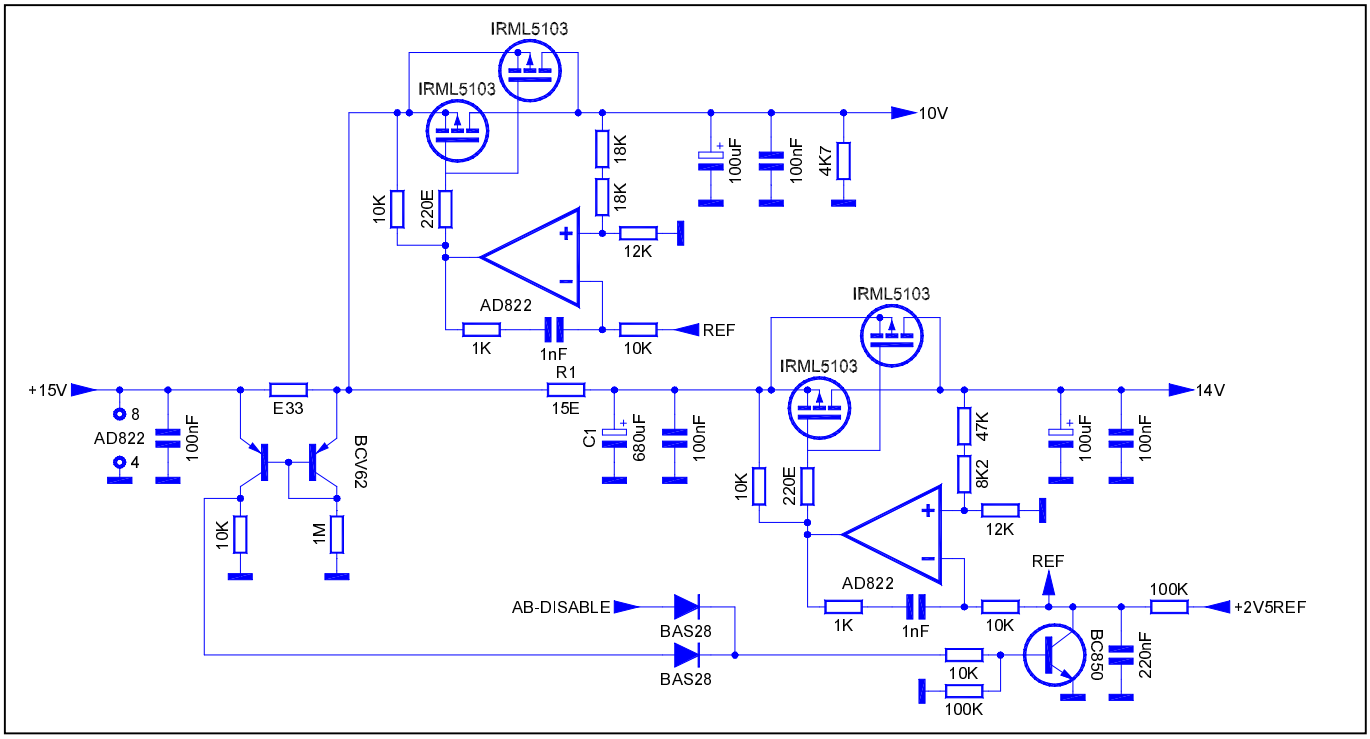


Figure 33: 10/14V Regulators

3.3.2 Horizontal Pulse Generator

3.3.2.1 Oscillator

Although any type of oscillator can be used, the best performance will be achieved using a transistor based crystal oscillator. Figure 34 shows an amplitude stabilized ground-base oscillator.

3.3.2.2 Duty Cycle Control

There are several reasons for the horizontal clocks to have a stable 50% duty cycle. In the first place this leads to the best possible overlap when transporting charges in the horizontal register. Furthermore, the pulses for correlated double sampling (CDS) are extremely important for obtaining the maximum performance. To obtain a stable duty cycle a control loop can be implemented as shown in Figure 35.

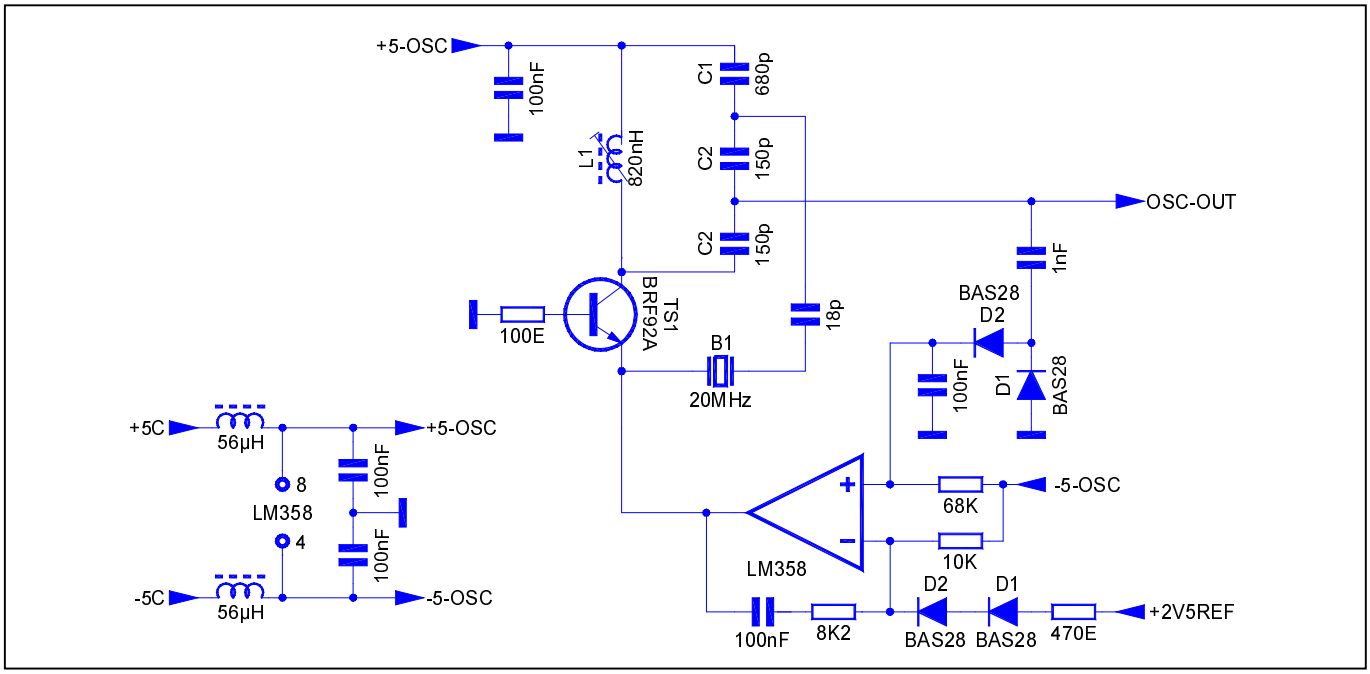


Figure 34: Crystal oscillator circuit

Since the collector circuit is tuned to the oscillation frequency, the crystal used can be a fundamental or overtone type. The peak value of the output signal is compared with a 2.5V reference voltage. The Op-Amp output controls the collector current through the transistor. The values are set to an output voltage of approximately $2V_{pp}$.

Design Considerations

The frequency dependent components are L1, C1 and C2 (2x). Optimum values can be calculated using the following formulas:

$$f = \frac{1}{2\pi\sqrt{L_1 \cdot C}} \quad \text{where} \quad C = \frac{\frac{1}{2}C_2 \cdot C_1}{\frac{1}{2}C_2 + C_1}$$

The ratio C1/C2 should be approximately 4½, but this value depends on the resistance of the crystal. With increasing crystal resistance, the ratio C1/C2 should be decreased. Fine-tuning the collector circuit (with L1) can be done by measuring the DC level on the output of the Op-Amp. The circuit is best tuned when the DC level is as close to GND as possible. The oscillator output should not be loaded with more than a single CMOS buffer.

To control the duty cycle, the DC level of the oscillator output signal is shifted so that the average DC level of the incoming CDS pulses is equal. Together with transformer TR5 in Figure 40 this assures a 50% duty cycle at all times.

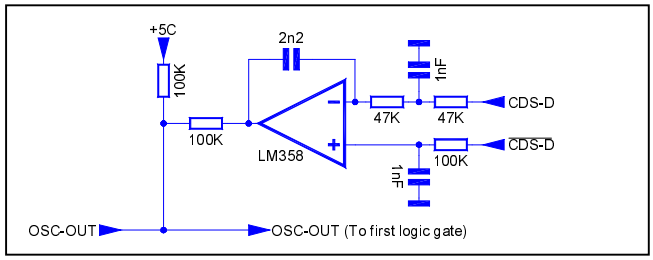


Figure 35: Duty-cycle control

3.3.2.3 *Horizontal Clock Shaping Logic*

Another critical part is the pulse generation logic. The circuit takes the oscillator signal as the input and generates the following signals:

- Horizontal transport gate clocks (PC1..3)
- Summing gate clock (PSG)
- Reset gate clock (PRG)
- Pre-processing clocks (PCDS and PCDSn)
- ADC clock (PADC)
- Output pixel clock (PXCLK)
- PPG clock

Figure 36 shows how the delays are created. The first gate buffers the oscillator output signal and transforms it into logic CMOS levels. Analog delay lines are used to create the necessary delay.

The values for delay lines DL1 and DL2 should be near 1/3th of the clock period. DL3 is used to compensate for the delay in the CCD output buffer.

The delay lines are driven with a series resistance equal to their characteristic impedance (in this case 100E). In each branch where no delay line is used a 100E resistor is used to compensate for the bandwidth loss of the delay lines in order to equalize the duty cycle. At 20MHz no capacitors need be used. When raising the frequency up to 30 or 40MHz they are necessary to lower the bandwidth.

Notice that each branch passes the same device. This ensures stable operation over a wide temperature range.

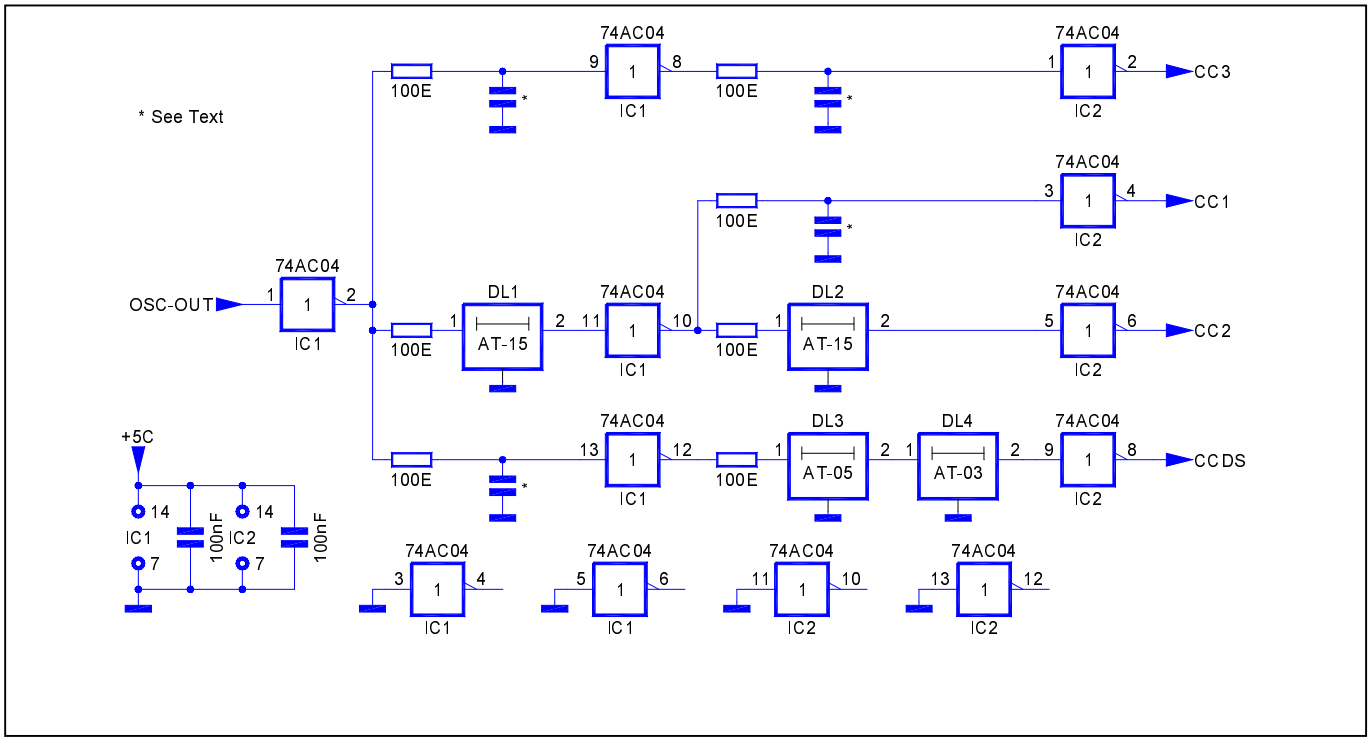


Figure 36: Horizontal pulse generation (part 1)

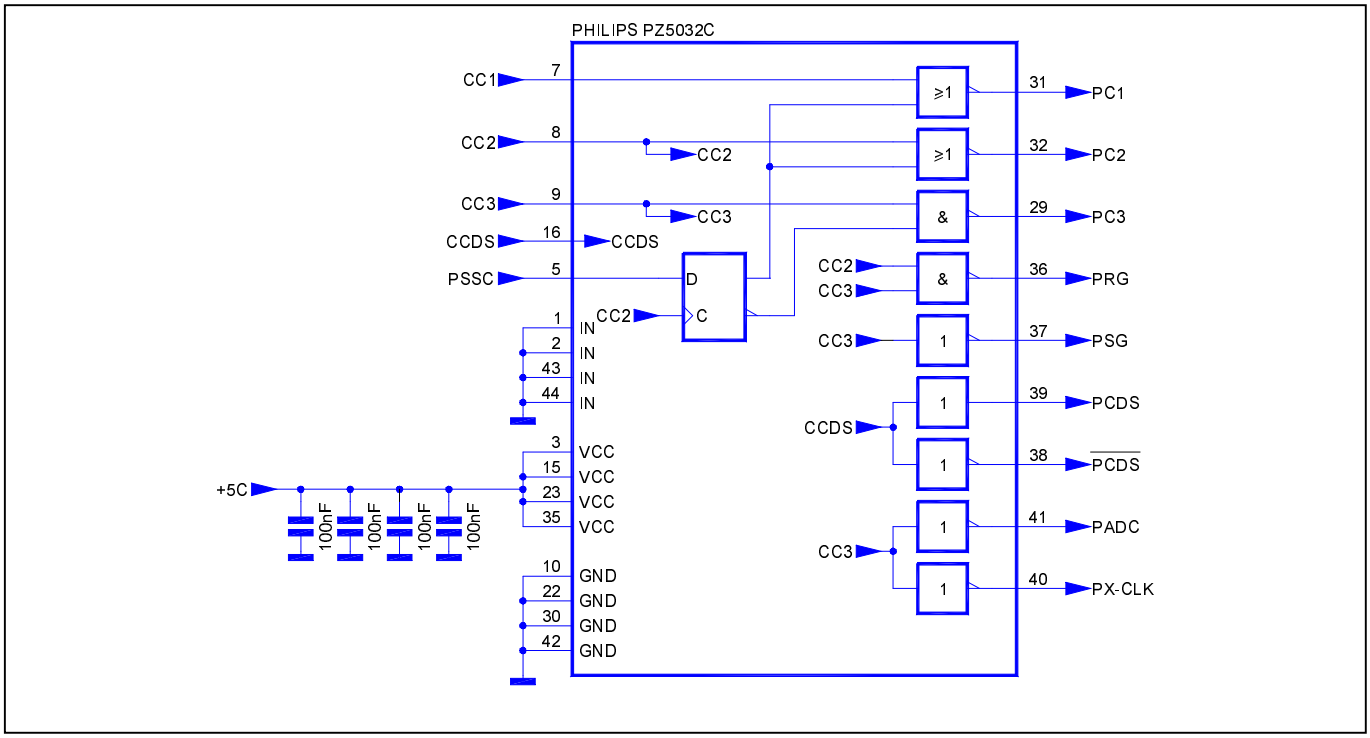


Figure 37: Horizontal pulse generation (part 2)

In the second part of the horizontal pulse generator the transport clocks (C1 to C3) are switched to a fixed level during the horizontal line blanking by PSSC. The reset gate is derived from CC2 and CC3.

For flexibility reasons the logic is implemented in a programmable logic device. This also has the advantage that all signals pass through the same device (for the same reason mentioned above).

To decrease the power consumption and to lower the cost price, the above circuit could be built using discrete (low voltage) logic.

3.3.2.4 *Horizontal Drivers*

All sensor related horizontal clocks are driven with AC logic buffer/inverters. To minimize undershoots and overshoots, the distance from the drivers to the CCD should be as short as possible. The following circuit shows the driver circuit for the horizontal register clocks (C1 to C3).

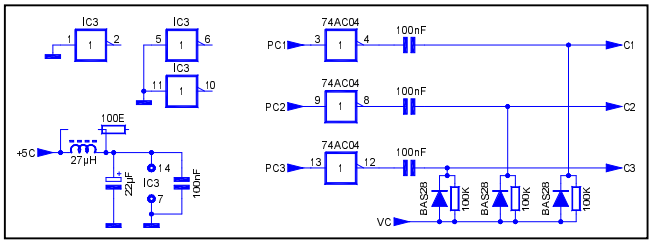


Figure 38: Horizontal clock drivers

When driving the FTT1010 at higher frequencies two buffers per gate are necessary to achieve the required minimum rise and fall times. The following table shows the number of AC logic buffers necessary for driving **each gate of a single horizontal register** (that is, W+X **or** Z+Y) of the FTT1010 or FTF3020.

	20MHz	36MHz	40MHz
FTT1010	1	2	2
FTF3020	3	6	-

The driver uses a separated supply (derived from +5C) to prevent cross-talk from and to other driver circuits (especially the RG/SG driver). The clocks are clamped to bias voltage VC.

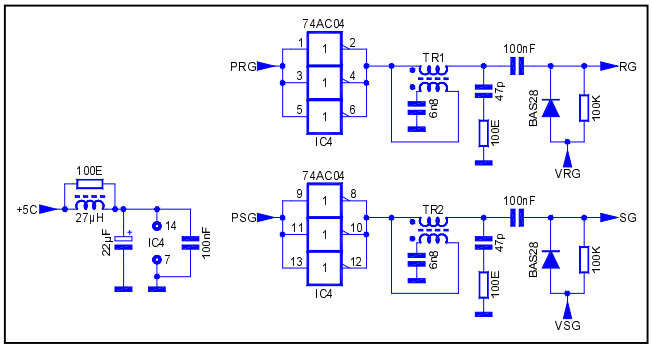


Figure 39: Reset Gate / Summing Gate drivers

The Reset Gate and Summing Gate not only need to be buffered; they must also be converted to 10V amplitude. A common-mode choke is used to double the output levels of the drivers. Refer to appendix 1 for type and manufacturer data of the common-mode chokes. The advantage of this circuit is that no separate 10V supply is necessary. On the other hand, it should be driven from a very low resistance source. This can be achieved using three AC logic buffers in parallel. The 6n8 capacitor prevents the drivers from being short-circuited when no clock is present. A terminating impedance minimizes the undershoots and overshoots. Remember that the values (47p and 100E) are valid for 20 MHz. The drivers are again separated from the +5C supply and clamped to the appropriate DC level. This driver should also be located as close as possible to the CCD. To maintain the timing relation among these signals over a wide temperature range all other horizontal clocks are led through the same driver device type. A single RG driver circuit can drive a single RG pin up to 40MHz or two RG pins up to 25MHz.

The CDS clocks are converted to 10V using the same principle as described above. Because the load of the CDS clocks is less than that of RG and SG, only two buffers in parallel are needed to drive the transformer. The two 10E resistors, in series with TR3 and TR4, limit the rise and fall times of the CDS drive pulses. To use this circuit at higher frequencies their values should be decreased.

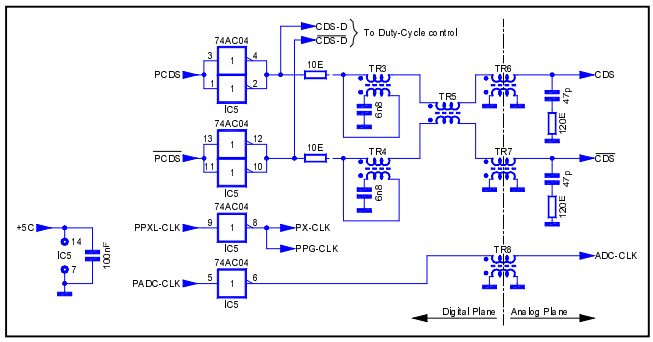


Figure 40: CDS clock drivers

TR5 forces both of the CDS signals to cross each other at the same time. TR6, TR7 and TR8 are necessary to cross from the digital to the analog (pre-processing) plane. Section 3.4 gives some guidelines for the PCB layout design of these critical clock signals. The termination networks must be at the end of the line (that is, where they are used in the CDS circuit).

3.3.3 Vertical Pulse Generator

3.3.3.1 Pulse Pattern Generator (PPG)

The PPG is the heart of the camera. It controls integration time and interfaces with the outside world. The following outputs are generated:

- Image clock driver inputs (PA1 to PA4)
- Storage clock driver inputs (for an FT CCD only; PB1 to PB4)
- Vertical clamp for black reference control (V-CLAMP)
- Charge Reset on VNS (NS-CR)
- A/B high-level and low-level switching (ABH, ABL, A-GND, A-LOW)
- Frame grabber control signals (H-Drive / V-Drive)
- Start Stop C (PSSC)
- Charge pump pulses for the 29V generator (SCP+, SCP-)

☞ *The pulse pattern of all sensor related outputs should match the latest data sheet to obtain maximum performance.*

Figure 41 shows an example of a PPG (which in this example is an FPGA). Since this FPGA is SRAM based, it needs to be loaded from a serial E²PROM (AT17C65) at power-up. To ensure proper loading and to prevent the FPGA from reaching a deadlock state, a watchdog/reset device (MAX823M) is used.

Besides the clock, an integration control (ITC) input can be applied to control integration time (and read-out). Figure 41 shows a mode input to switch between for example, binning and normal read-out mode. Both ITC and MODE are external inputs and should be protected against ESD destruction as shown in the figure.

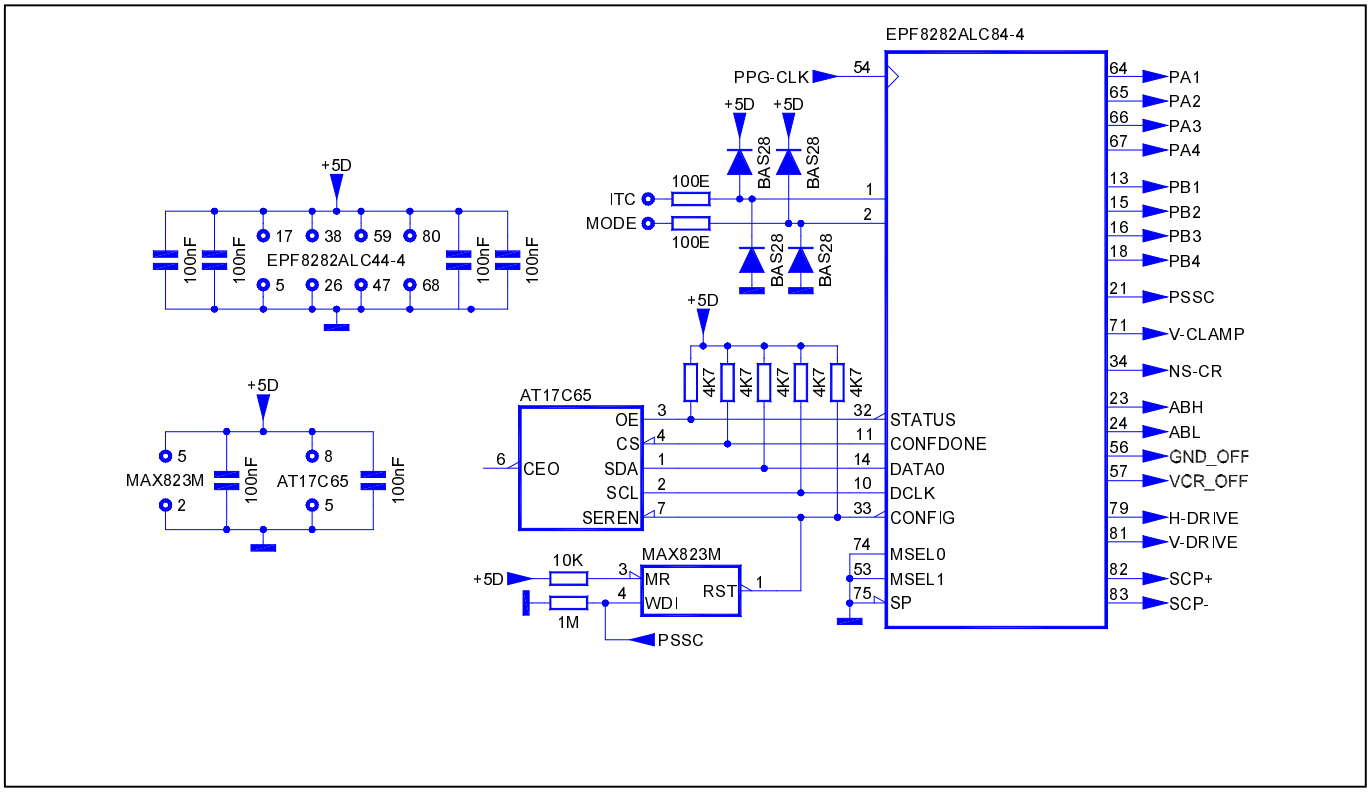


Figure 41: Pulse Pattern Generator

3.3.3.2 High-level and Low-level Switches

In order to obtain the specified sensor performance it is necessary to switch the high levels of the image and storage gates (see also section 1.2.3). Figure 42 shows the high level switch. Four low On-Resistance MOSFETs are used to switch the positive driver voltages between 10V and 14V. Two MOSFET drivers that accept TTL levels, drive the switching MOSFETs. Each switch is separately controlled by the PPG.

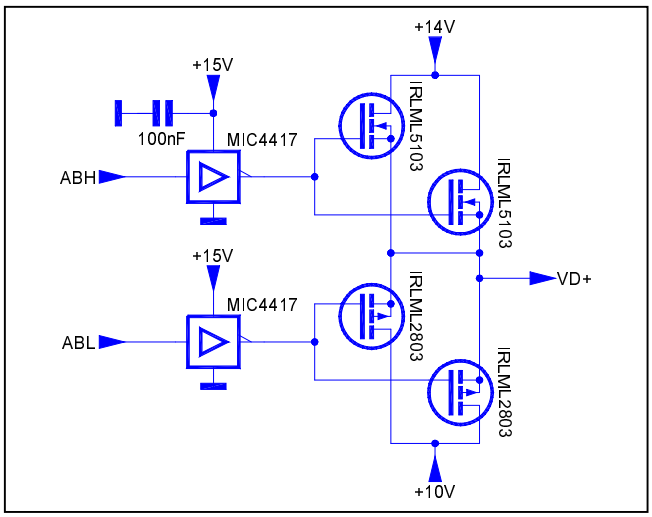


Figure 42: High-level switch

Section 1.1.4 explains two charge reset methods. If the image gates need to be switched to the charge reset level, a 4-level clock is necessary. In this case the circuit in Figure 43 can be used to switch the low driver voltages between GND and VCR (-5V).

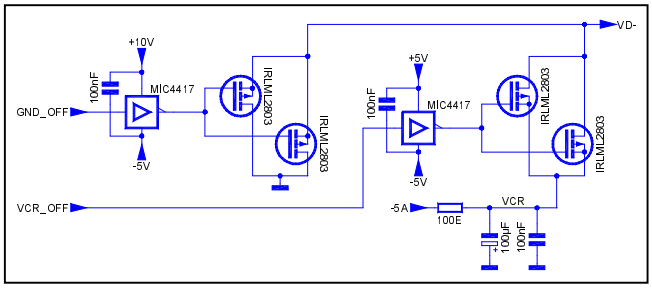


Figure 43: Low-level switch

Design considerations

Each switch is built with two low On-Resistance MOSFETs to obtain short switching times and to minimize switching losses. For the same reason two separate MOSFET drivers are used. This also has the advantage of controling the time between one MOSFET pair switching off and the other pair switching on, so avoiding cross conduction.

3.3.3.3 Vertical Drivers

Depending on the charge reset method (described in section 1.1.4) a 3-level clock is the minimum configuration. With this configuration a charge reset pulse must be added to VNS. Only the high level needs to be switched. Figure 44 shows an example of the image gate drivers in a 3-level clock configuration.

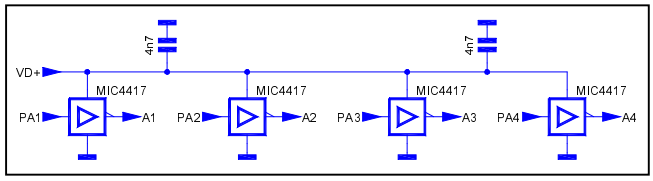


Figure 44: Image gate drivers (3-level clock)

Inputs PA1to PA4 are TTL level signals that come from the pulse pattern generator. VD+ is switched between 10V and 14V. To ease switching of the high levels, the values of the two by-pass capacitors should not exceed 4.7nF.

If the low level needs to be switched, then the circuit in Figure 45 can be used. When VD- is connected to GND the outputs switch between GND and VD+. If VD- is –5V all driver outputs are automatically switched to –5V because the inputs are logical high compared to –5V.

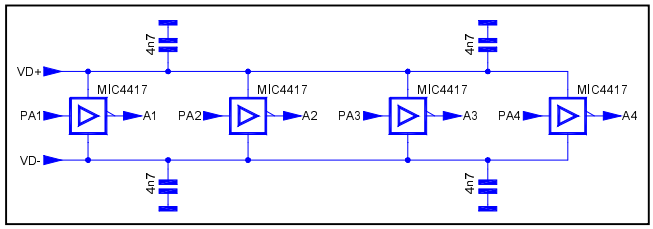


Figure 45: Image gate drivers (4-level clock)

The storage gates don't need to have a 4-level clock because no charge reset is performed on the storage section. A 3-level clock is necessary to be able to handle the Qmax during vertical transport.

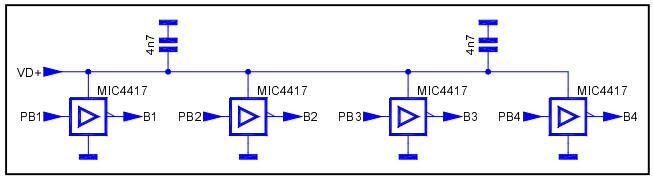


Figure 46: Storage gate drivers (FT only)

3.3.4 Protection Circuits

There are two reasons for using protection circuits in a camera:

1. *Protection of the CCD*
   First of all, several measures must be taken to ensure the CCD won't be permanently damaged in the application. If no protection is used, the probability of damaging the CCD is high (for example, when switching the power-supply on and off). There are several precautions necessary to guarantee maximum safety.
   Some of the bias voltages should be protected against unwanted potential differences. Section 3.3.1.3 tells how to avoid unwanted potential differences by simply adding 4 Schottky diodes.
   Another sensitive part of the CCD is the output buffer. Avoid exceeding the maximum specified current. Also, never use a separate supply for the first buffer and the output buffer of the CCD (named SFD). Use the same supply for each output. Section 3.3.5.1 outlines the right configuration.
   Make sure that each bias and supply voltage for the CCD is current protected.

2. *Protection of the camera electronics*
   There is no way to build a reliable application without any protection circuitry. Not only does the CCD have to be protected but also the driving electronics. In case of a short circuit some measures should be taken to keep the camera alive.

The DC bias supplies are described in section 3.3.1. Figure 47 shows how these blocks are connected to obtain a robust protection scheme.

Both the 29V supply and the SFD regulator have a short circuit detection output. These outputs (29V-LIM and SFD-LIM) are input to the PPG via a wired OR. If any of them becomes active the SCP switch is disabled, resulting in a lower output voltage of the 29V generator. Also, the 10/14V regulators are disabled via a second OR port inside the PPG. This causes the vertical gate drivers to be disabled. As soon as the 29V drops below ±15V these are also shut down. This is useful in case the regulator is defective.

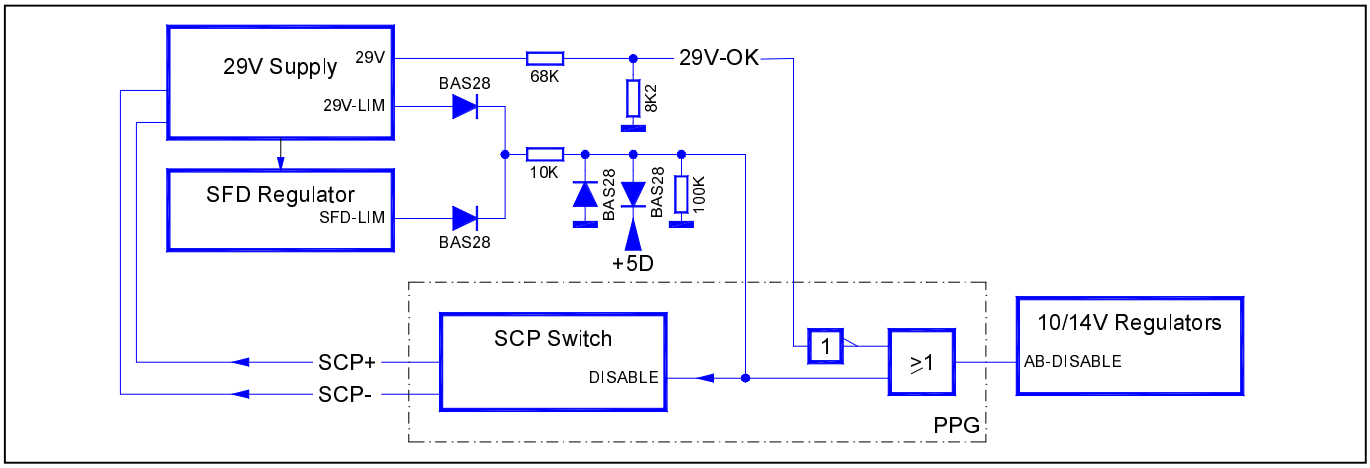


Figure 47:Protection circuits block diagram

3.3.5 Pre-processing

The purpose of the pre-processing circuit is to demodulate the CCD output signal to make it suitable for feeding an A/D converter, and to suppress the 1/f and reset noise. The black level also needs to be clamped to a reference level to get the maximum dynamic range. The art of building a good pre-processor is to find the best compromise between excellent pixel separation and good noise performance. Good pixel separation means that the output signal of each pixel is not affected by its neighbours. This paragraph shows a 20MHz CDS circuit that can easily be scaled for higher frequencies.

3.3.5.1 CCD Output Buffer

The CCD output buffers have an open source output and should be loaded with a resistor to GND. In order to prevent bandwidth limitation as a result of capacitive loading, an emitter follower with a high-frequency transistor should be used (as shown in Figure 48). It is essential to mount the emitter follower (including by-pass capacitor) as close as possible to the output pin.

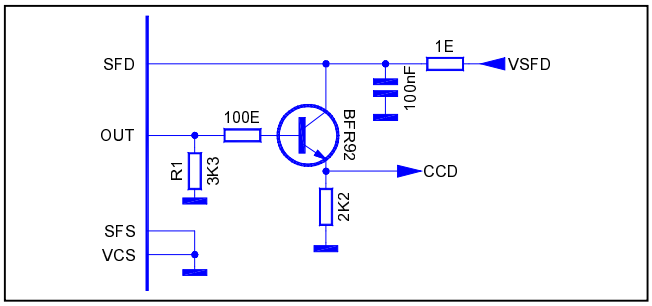


Figure 48: CCD output buffer

The bandwidth of the output buffer is determined by the load resistor of the output buffer (R1). In most applications a 3K3 resistor will do. At higher frequencies more bandwidth may be necessary. This can be achieved by decreasing the value of R1 to 2K2.

The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed.

☞ *Measuring directly on the output pin of the sensor with an oscilloscope probe can easily damage the output buffer. To avoid this, measure on the output of the emitter follower instead.*

3.3.5.2 CDS Circuit

There are several ways to process the CCD output signal. A Correlated Double Sampling (CDS) pre-processor is a very popular type. For low-end applications CDS chips are widely used (and are often integrated with an A/D converter). Since these chips in general are limited to 10 bits performance and about 25MHz clock-frequency, this reference design uses a discrete built CDS pre-processor. This has the advantage of being able to scale the circuit up to 40MHz. Another advantage is that we can use 50% duty cycle clocks instead of 25% in low-end CDS chips, resulting in lower read-out noise (especially at higher frequencies) and thus a higher dynamic range.

Figure 49 shows the discrete CDS solution. As mentioned before, all component values are tuned for a clock-frequency of 20MHz. The overall gain is set so that the maximum linear range of the CCD matches the A/D converter range (in this case 0.25V to 4.25V).

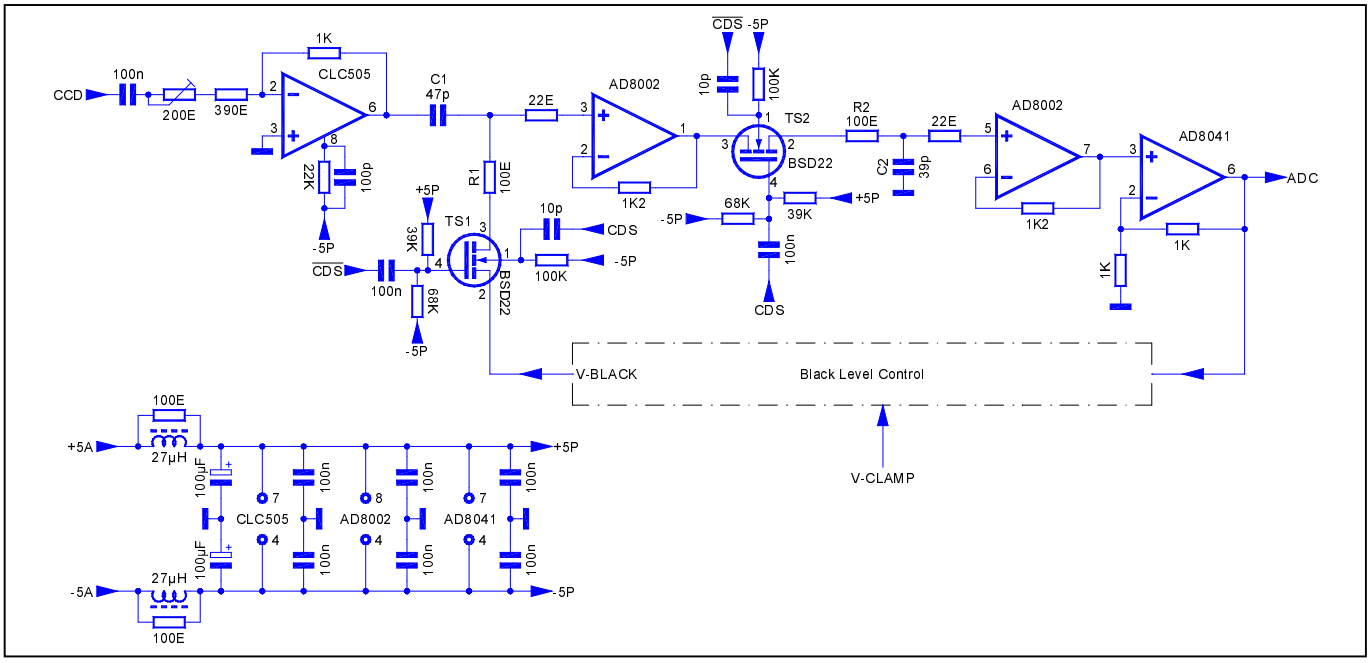


Figure 49: CDS Pre-processor

The first Op-Amp (set at ±3dB gain) buffers the AC coupled CCD signal for the first part of the CDS. The first FET clamps the reset hold level of the CCD signal slowly to V-BLACK (see the following paragraph). This clamp also removes the 1/f noise component. The second Op-Amp is a unity-gain buffer feeding the sample and hold circuit. During the active pixel time the second FET loads the capacitor C2 with a speed determined by R2. The values of R2/C2 determine the performance of the CDS circuit. High RC values lead to bad pixel separation and good noise performance while a low value has the opposite effect. As mentioned before, the best performance can only be a compromise of these two parameters. The clamped video signal is buffered by a second wide-band Op-Amp. The last Op-Amp (AD8041) drives the A/D converter.

Design considerations

The first buffer should have sufficient bandwidth (at least three times the pixel frequency) since the reset cross-talk should be amplified undistorted. The product of (R1+R_{on}) and C1 should be approximately 1/6th of the pixel-time (R_{on} of the BSD22 is about 40E). The product of (R2+ R_{on}) and C2 should be 1/10th of pixel time. Capacitor C1 should not be chosen too low because otherwise stay capacitance to ground will result in a loss of performance. For this reason it is recommended that the ground plane underneath the connection of C1, R1 and the 22E resistor (especially at higher frequencies) be removed.

3.3.5.3 Black Level Control

Control of the black level can be achieved in two ways. The first method uses the black columns. Because the clamp circuit has to be settled in 20 pixel clock-cycles this requires a fast clamp, which results in line noise. The second, and preferred method, uses the black line that first comes out of the CCD. At the start of each field this line is clamped to the preset video black level. During read-out of the field the black level is stable (assuming no leakage of the hold capacitor).

(Some applications require a black level setting that isn't equal to the black level of the CCD. Instead, a zero-level dark current level is necessary. This can be achieved by reading out an empty line from the horizontal register before the start of read-out and then clamping to this line.)

The ADC input signal passes a low-pass filter (R1/C1) and an AD706 buffer. During the black line (when V-CLAMP is high), TS1 is switched on. Capacitor C1 is charged until the level at the inverting input reaches the preset black level. At the end of the black line TS1 is switched off. Capacitor C2 holds the black level during read-out of the field. Because of the heavy load of the black level control circuit, a video Op-Amp is used as buffer.

Design considerations

The first low-pass filter makes the high frequency signal suitable for the AD706, which is a low frequency Op-Amp. The time constants R1/C1 and R2/C2 should be chosen in such a way that the black level can be settled within one active line-time. The values of Figure 50 are valid for an FTT1010 application running at 20MHz using a single output. Capacitor C2 should not be chosen too small since this would cause too much leakage current from the Op-Amp at higher temperatures, which results in a vertical shading of the image.

When designing an application which supports single shot modes, the V-CLAMP should be activated only when the CCD is idle (that is, when no picture is read out) to prevent the black level from drifting away.

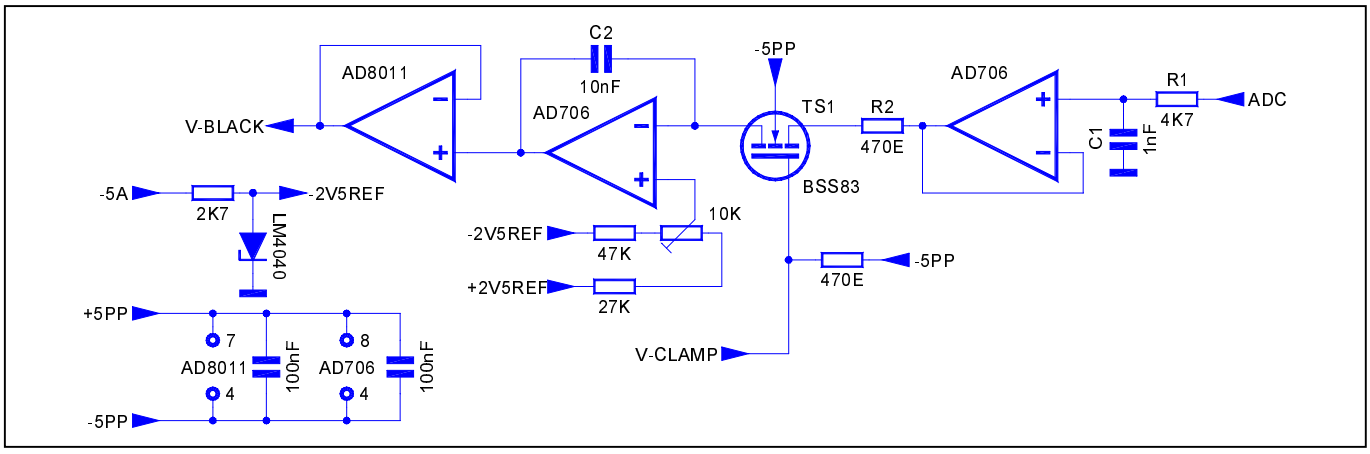


Figure 50: Black level control

3.3.6 A/D Converter

The final analog part of the camera is the A/D converter, which converts the discrete time video signal to a 12-bit digital signal. Figure 51 shows the circuit of the A/D converter that operates in single ended mode, using its own internal voltage reference. The input range is from 0.25V to 4.25V.

The low-pass filter at the ADC input prevents high frequency components from being sampled, which reduces the amount of noise. The ADC type has an integrated track and hold circuit, which starts converting at the falling edge of the CLK input.

HC logic devices buffer the digital outputs before they are distributed to for example, a frame grabber. For optimum performance, place the buffers near the A/D converter. This example shows single ended digital outputs. There are a lot of circumstances however, where differential outputs are required (when using long cables at higher frequencies).

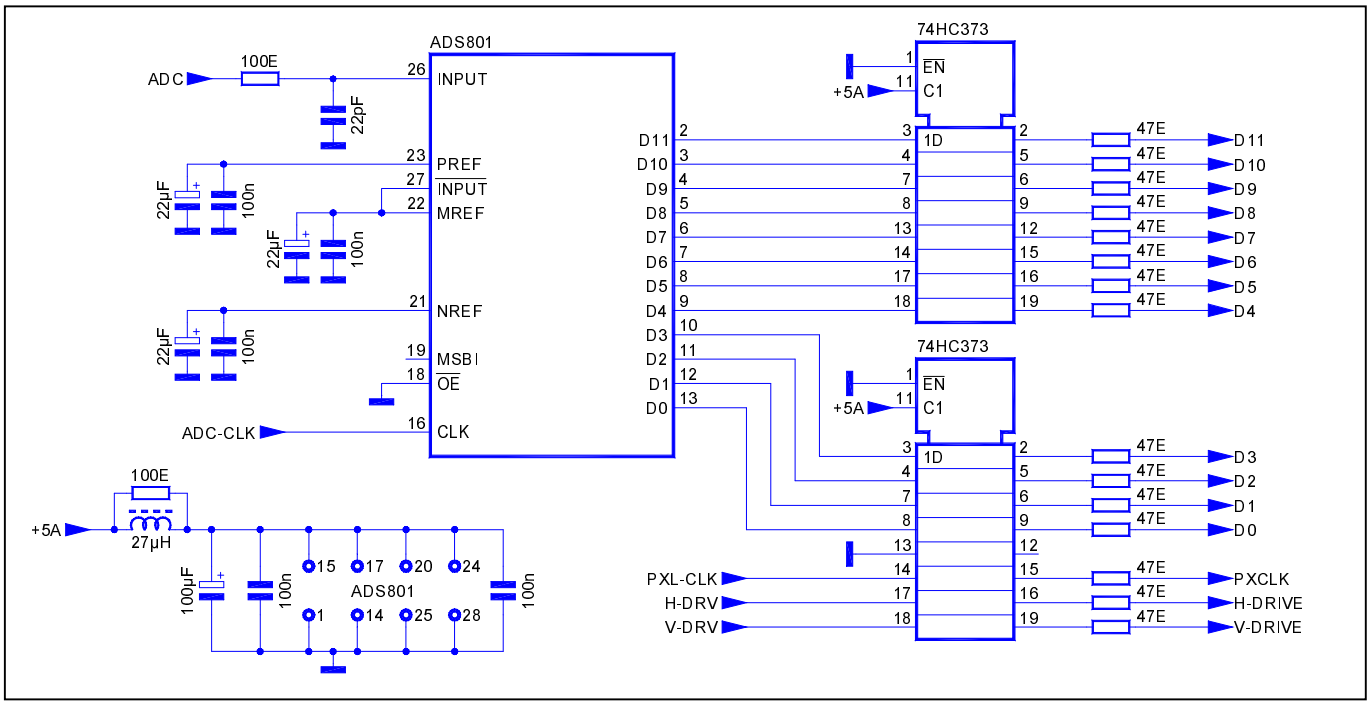


Figure 51: A/D Converter

3.4 Layout Design

Now that all the schematics are known, it is important to design a proper PCB layout. This note assumes that anyone who is going to design a CCD camera is aware of all PCB layout design rules and general EMC precautions that are necessary in a mixed signal environment.

First of all, a proper designed ground plane is the foundation for a good quality PCB design. It prevents cross-talk from the (digital) noisy neighborhood into the sensitive analog electronics. Figure 52 gives an overview of a ground plane and some functional parts.

Three planes can be identified. The first one to be separated is the analog pre-processing plane. There are just a few ground connections with the other planes. The first connection is at the position where the buffered CCD signal enters the pre-processing input. The other connection is underneath the A/D converter. The second plane that is separated is the horizontal pulse generator plane. Separating this plane decreases the chance of cross-talk from vertical digital signals that might result in phase modulation of the horizontal clocks which will definitely become visible in the output signal. This plane is connected to the outside world plane underneath some of the clock outputs. All the less critical circuits are located on the third plane.

Another important issue is the power supply distribution and by-passing. Never use a single regulator to supply the analog and digital electronics. The horizontal and vertical digital supplies can be derived from the same regulator, but should be separated by an inductor and a ceramic and electrolytic capacitor. Don't try to cut down the camera cost price by using capacitors with high ESR values. This will degrade the overall performance.

Common mode chokes should be used to control the return currents of the CDS and ADC clocks. As shown in Figure 52, the return traces are connected to the plane near the position where the clock signal is used. The CDS signals are terminated with a series impedance as close as possible to the gate of the FET (pin 4). The placement of some parts is also a point of attention. The CCD output buffer (emitter follower) should be mounted as close as possible to the CCD output pin. If possible, the pre-processing circuit must be placed directly after the output buffer. If this cannot be done a common mode choke must be inserted between the CCD output buffer and the pre-processing input. The importance of good power supply by-passing has already been mentioned. The same arguments are valid for by-passing the reference input of the A/D converter.

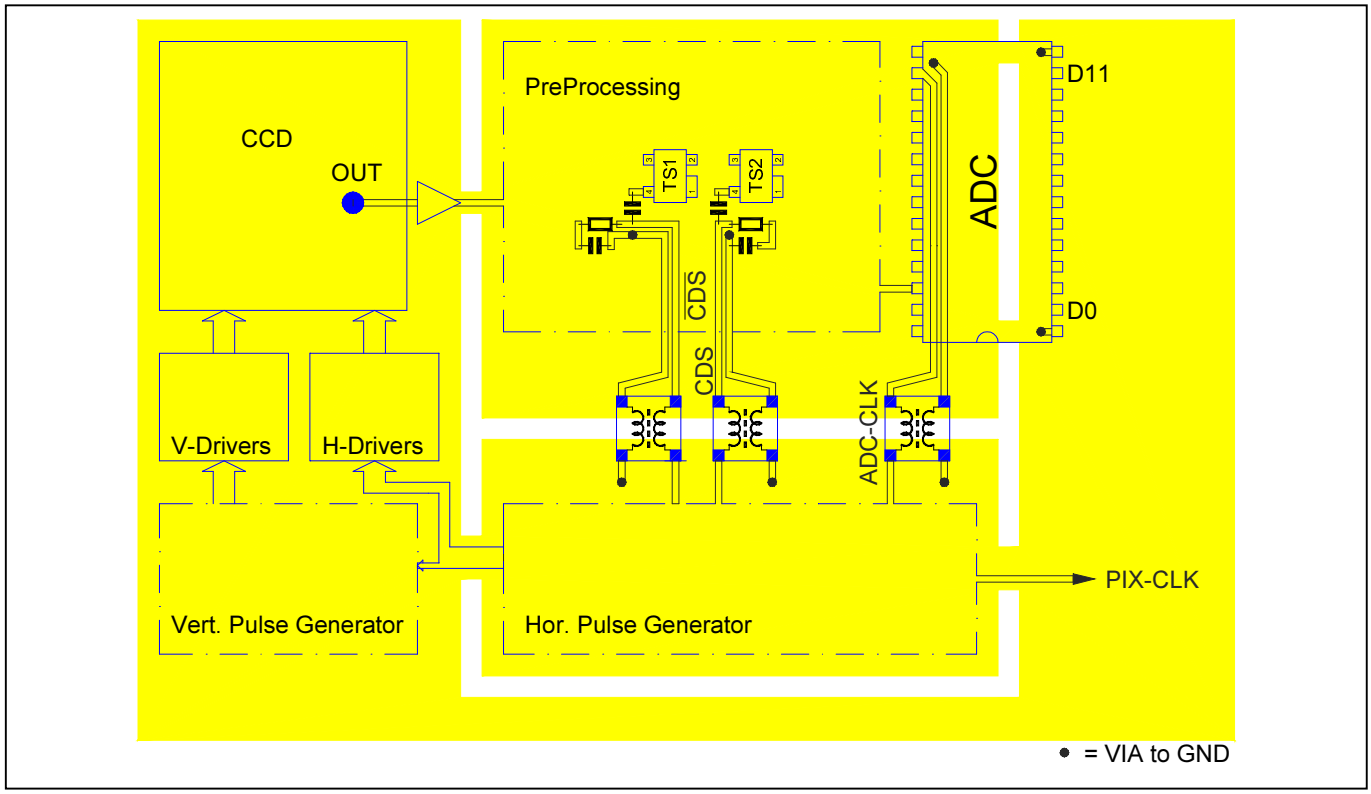


Figure 52: Ground Plane and clock distribution

4 Golden Rules

To successful design a high performance CCD camera one must be aware of the following rules.

- Make sure you fully understand the operation of the CCD including the function of each pin.
- Consider all of the horizontal clocks as analog circuits since any noise on these signals will be visible in the output signal. This means that phase noise caused by cross-talk of any other signal (especially with a lower frequency) should be avoided. For this reason it is recommended that the horizontal clock circuitry is isolated from the rest of the electronics.
- Make sure the rise and fall times of all transport clocks (both horizontal and vertical) are fast enough. Too slow clock drivers result in a too short overlap time. This leads to a deterioration of the charge transport efficiency, yielding a lower Qmax. Typical effects of slow horizontal clock drivers are bad pixel separation or vertical stripes.
- Don't re-invent the wheel. Many engineers have spent years on developing high performance cameras. This has resulted in a camera set-up as presented in this note. Of course, one is free to use other circuits or components, as long as it basically has the same functionality.
- Protecting the camera from unwanted differential voltages is an essential part of a camera design (see also section 3.3.4). Be aware of the safe startup sequence of all CCD signals. Here's the sequence:
    1. VNS
    2. VSFD
    3. the rest

  This does not mean that VNS should be stable before VSFD can be switched on. As long as the VNS voltage is a minimum of 1V higher than VSFD. Deriving all sensor bias DCs has the advantage that this law isn't violated. When switching off the camera, remove the signals in reverse order.
- Be sure you read the section on layout design. No matter how good your schematics are, a poor layout design will definitely lead to a disappointing performance.
- The performance figures are valid for the typical values mentioned in the data sheet. To obtain maximum performance use the specified bias voltages and waveforms.
- In most cases only one output register and one output buffer is used. The **unused output buffers and output register** pins should be connected as follows for safe operation:

Pin	Connected To
RG	Reset Drain voltage (+15V)
SG	GND
C1..3	GND
VCS	-5V (preferred) or GND
RD	Reset Drain voltage (+15V)
SFD	VSFD
SFS	GND
OG	VOG
Output	Not Connected

5 Appendix 1: Component Listing

Name	Manufacturer	Type Number
Electrolytic capacitor 100µF/16V	Sanyo	16CV100GX
Electrolytic capacitor 10µF/35V	Sanyo	35CV10GX
Electrolytic capacitor 47µF/35V	Sanyo	35CV47GX
Electrolytic capacitor 22µF/35V	Sanyo	35CV22GX
Electrolytic capacitor 220µF/6V3	Sanyo	6CV220GX
Electrolytic capacitor 10µF/63V	Philips	2222 036 78109
Electrolytic capacitor 68µF/63V	Philips	2222 036 38689
Chip Capacitors	Philips	
Chip Resistors	Philips	
Micro chip inductor 12 µH PM10	TDK	ACL3225S-120K-T
Micro chip inductor 27 µH PM10	TDK	ACL3225S-270K-T
Micro chip inductor 56 µH PM10	TDK	ACL3225S-560K-T
Crystal 20MHz 49SMLB	Saronix	
Common mode choke	TDK	ACM3225-102-2P-T
Adjustable coil 820nH 5CCE	Toko	638AN-0163Z=P03
Analog delay line 3ns/100E	Showa	AT-03
Analog delay line 5ns/100E	Showa	AT-03
Analog delay line 15ns/100E	Showa	AT-15
Hex Inverter	National	74AC04SC
Quadruple latch	Philips	74HC373D
Op-Amp CLC505	ComLinear	CLC505AJE-TR13
Dual LF Op-Amp AD706	Analog Devices	AD706JR
Dual LF Op-Amp AD822	Analog Devices	AD822AR
Op-Amp AD8011	Analog Devices	AD8011AR
Op-Amp AD8041	Analog Devices	AD8041AR
Op-Amp AD8002	Analog Devices	AD8002AR
Op-Amp LM358D	Philips	LM358D
Op-Amp TL082D	Thomson	TL082CDTS93
Precision voltage reference LM4040	National	LM4040 CIM3X-2.5
P-channel MOSFET	IR	IRLML5103
N-channel MOSFET	IR	IRLML2803
A/D Converter	Burr Brown	ADS801U
MOSFET Driver	Micrel	MIC4417BM4
CoolRunner PLD	Philips	PZ5032C
FPGA	Altera	EPF8282ALC84-4
FPGA Configuration E²PROM	Atmel	AT17C65-10PI
Reset Watchdog Circuit	Maxim	MAX823MEUK
5V1 Zener Diode	Philips	BZX84-C5V1
BAS28 Diode	Philips	BAS28
BAT74 Diode	Philips	BAT74
BFR92 Transistor	Philips	BFR92
BC850 Transistor	Philips	BC850
BC860 Transistor	Philips	BC860
BSS83 Transistor	Philips	BSS83
BSD22 Transistor	Philips	BSD22
BCV62 Transistor	Philips	BCV62
BST120 Transistor	Philips	BST120